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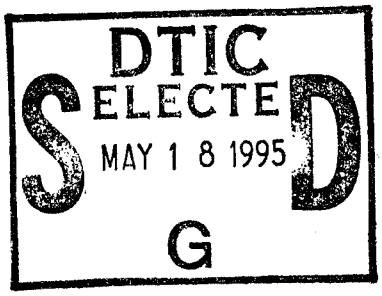
SELF STRESSING TEST STRUCTURE CELLS

University of Southern California

Vance C. Tyree



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APPROVED: Steven L. Drager

STEVEN L. DRAGER
Project Engineer

FOR THE COMMANDER: John J. Bart

JOHN J. BART
Chief Scientist, Reliability Sciences
Electromagnetics & Reliability Directorate

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6. AUTHOR(S)

Vance C. Tyree

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

University of Southern California
Information Sciences Institute
4676 Admiralty Way
Marina Del Rey CA 90292-6695

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13. ABSTRACT (Maximum 200 words)

This report addresses the work performed to design on chip reliability prognostics for purposes of monitoring fielded integrated circuits for degradation due to the failure mechanisms of oxide breakdown, electromigration, and hot carrier degradation. The self stressing test structure cells are self-contained standard cells that include the test structure, stressing, and monitoring curcuitry and a boundary scan interface to be used with the IEEE 1149.1 boundary scan Test Access Port. The cells have been designed to work within the limitations of a CMOS integrated circuit, i.e., no additional power levels are needed, the cell area has been kept as small as possible, the cells may be incorporated independently from active circuitry, and cells will not degrade chip lifetime. The self stessing cells have been shown to function by simulation, but further study to correlate cell degradation to integrated circuit degradation is required.

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Self Stressing Test Structure Cells

Summary:

It is widely recognized that there is serious need for determining the probable lifetime of application specific integrated circuit (ASIC) designs by using wafer level reliability (WLR) testing at the wafer fabrication line either during wafer fabrication (in-process testing) and/or after full wafer processing. The in-process WLR testing and post-processing WLR testing are becoming a normal part of quality wafer fabrication partially because of the market place need for higher reliability and quality. In addition, with the new QML (MIL 38535) procedures that are now becoming a standard part of the military ASIC acquisition requirements, the need for WLR testing is a standard assumption at QML qualified ASIC manufacturers. All of this attention to wafer fabrication is extremely important to the maintenance of ASIC quality, but little has been done to assess the reliability impact that result from changes in mechanical, thermal, and electrical stress that ASIC parts are subjected to after they are installed in the target systems.

In order to provide insight into the effects of ASIC packaging and ultimately, system packaging, a means is needed to be able to view the packaging environment as part of the overall reliability assessment of the ASIC parts. One method for providing the needed visibility into the packaging environment is to create a library of test structures that can be installed into ASIC systems along with the primary functional circuitry to provide access to reliability limiting mechanism characteristics through the host system diagnostic capability that is a natural extension of system testability requirements. This library of reliability test structures should also provide the means for evaluating packaging stresses without having the complexity and cost of the final ASIC chips involved in the package reliability tests by offering simple methods for creating reliability test chips for package environment testing.

The goal of this work was to develop a library of reliability test structures that are capable of performing accelerated reliability tests similar to the type of tests conducted at wafer level for the WLR testing at the end of wafer fabrication. These test structures will be capable of conducting reliability tests that assess electromigration (EM) performance of all layers of metal, time dependent dielectric breakdown (TDDB) tests on gate insulators, and hot carrier damage (HCD) rates on minimum channel length transistors while providing for digital access to setting stress conditions, failure criteria (where appropriate), and reading the number of failed structures or devices. It is desirable to have the cells constructed in accordance with the physical and

electrical interface constraints of a DoD CMOSN standard cell library to enable incorporation of reliability test structures in systems while using existing design tools. Another goal of this work was to include the reliability test cells into the control chains used by ANSI/IEEE Std. 1149.1 boundary scan (Test Access Port: TAP)[1] and common built-in-test architectures to track reliability limiting processes in normal system operation or into simple specialized reliability test chips for monitoring and evaluating new packaging environments.

Self-stressing structures designed under this task were limited to the three mechanisms most commonly discussed in the literature. Also, they reflect the current thrust of the JEDEC standards activity. Two primary goals of this work were:

1) Define the specific reliability structure layout to implement EM, stress migration (a sub-function of the EM test structure), TDDB, and HCD monitoring requirements with stress control and monitoring capability that is suitable for normal burn-in and life testing stress acceleration factors. The range of available stress conditions will be constrained by available standard power supply voltages used by the ASIC's, so the practical limits on acceleration factors will be defined in this effort.

2) Define digital control and monitoring interfaces that are accessible from a standard TAP interface. This includes defining the built-in-test design strategy rules for constructing the TAP interfaces with the CMOSN Standard Cell Library.

The TAP interface that was actually designed for demonstrating the self-stressing cells used a very simple architecture that would adequately demonstrate the cells, but would likely not be actually used in a typical ASIC boundary scan. We believe that since the self-stressing cells are rather simple in their control architecture there would be no difficulty in installing them within any ASIC boundary scan architecture. This choice also greatly simplifies the demonstration of the cells in simulations and in test chips.

All of the self-stressing test structures were designed with the assumption that there would be only a single power supply potential available in a typical ASIC. This placed severe constraints upon the implementation of monitoring electronics because the monitoring functions are basically analog. It is rather difficult to implement analog to digital (A/D) converters with only a single power supply. It is necessary to sacrifice many of the simple quantitative voltage and current measurements that one would desire in order to operate in a 5.0 Volt single power supply chip. Many of the test results can be expressed in terms of a fail, not-fail indicator. In some cases, as in the case of hot carrier damage, an indication of relative change is mandatory. In order to satisfy that need a crude A/D converter was designed using a Current Controlled Oscillator. The design chosen is sufficiently linear to be capable of distinguishing differences

[1]ANSI/IEEE Std. 1149.1, IEEE Standard Test Access Port and Boundary-Scan Architecture (SH 13144).

between a device under stress and a reference device (unstressed) to an accuracy of about eight bits. By using an unstressed test structure as a reference is was not necessary to design an A/D converter that was stable over temperature. The only requirement is that it must be linear to an accuracy of about 1% or better.

A test chip was implemented to test some of the basic structure functions but the chip was not functional because there was a significant layout incompatibility between the CMOSN standard cells used in part of the chip and the circuits designed using MOSIS Scaleable CMOS rules. There was not sufficient time to implement a second test chip and test it within the time frame of this work. This report contains only SPICE simulations of the test structures. In the one case where a test chip would have been most beneficial (the hot carrier damage test structure) we were able to extract SPICE model parameters from devices that had been exposed to varying amounts of hot carrier stress. The resulting simulations should accurately reflect the actual test chip behavior of the HCD test structure.

Each basic self-stressing test structure cell has been carefully simulated, including all supporting circuitry, including the boundary scan cells and the current controlled oscillator. In addition, a representative sample of the self-stressing cells were assembled into a test chip and simulated. Even though the test chip has not been fabricated we are confident that the test chip would perform as predicted if it were fabricated.

The main body of this report contains a detailed description of the circuit designs of the test structures and the simulations that were used to verify their functionality. It is possible to fabricate a test chip to demonstrate the self-stressing test structures by simply submitting the geometry file contained in the tape cartridge that is included with this report.

Design Constraints:

The primary requirements set for this self-stressing test structure cell library is that they must be constructed with a form factor that will permit their assembly using commercial CAD tools. The DoD CMOSN cell library was chosen for the digital cells for the control logic, so the cell pitch for this library was arbitrarily chosen for the self-stressing test structure cell size. All control logic necessary for the Boundary Scan interface and the test structure control logic must be assembled from the CMOSN cell library.

The stress conditions for the cells must be adjustable within reasonable limits set primarily by the limitations imposed by a single 5.0 Volt power supply. In addition, power dissipation in the electromigration test structure placed limitations on the maximum stress current that could be applied to the electromigration test structure. The 5.0 Volt power supply limit also placed constraints upon how much stress could be applied to the gate insulator. A relatively modest

stress field can be generated by implementing a well bias generator for each TDDB test capacitor included in the test chip. A well bias generator is capable of producing an effective increase in stress voltage of the order of 1 to 2 Volts.

In general the philosophy was that the self-stressing test structures should operate at slightly higher stress than is normally applied in normal chip operation. This slightly greater stress will create failure rates in the test structures that is significantly greater than normal operation, but not so large as to potentially stimulate secondary failure mechanisms. It was desirable to provide an "early warning" failure rate for monitoring ASIC devices. A significant number of test structure failures should occur comfortably before expected failures of the ASIC device itself. The "early warning" feature will be useful for both burn-in testing and for monitoring failure rate due to various mechanisms while an ASIC is in service. Scheduled repair of electronic systems can be defined by selecting a particular failure rate for the test structures on an ASIC device and then scheduling ASIC replacement after the selected test structure failure rate is exceeded.

Cell Design Descriptions

There are five cells which will be described in this document. The first is the Current Controlled Oscillator which serves as the system analog to digital converter that operates within the confines of a single power supply voltage of the chip while providing a large dynamic range relative measurement of current changes. The next three cells, Time Dependent Dielectric Breakdown, Hot Carrier Damage, and Electromigration, are the reliability monitoring cells of the system that have both stress control and structure degradation measuring capability. Lastly, the Boundary Scan Interface and Cell Controller are discussed which provide a simple demonstration interface between the reliability monitoring cells and the ANSI/IEEE Std 1149.1, IEEE Standard Test Access Port and Boundary-Scan Architecture.

Current Controlled Oscillator:

A simple method for digitizing the analog quantities that reflect the state of the self-stressing test structures at various time intervals was needed. Many different analog-to-digital converter designs were reviewed and rejected because all of them require a dual power source with an operating voltage of ± 5.0 Volts or greater. Since an additional power supply voltage was specifically disallowed in this task we considered using smaller voltages with an internal synthetic ground that gave us the equivalent of ± 2.5 Volts. Unfortunately this strategy gave us a very limited dynamic range that was useless for testing the self-stressing test structure that required a large dynamic range (specifically the Hot Carrier Damage test structure). Fortunately neither high precision nor high linearity were required for this application.

Since voltage measurement without dual power supplies was ruled out we settled upon a current mode measurement strategy. The Hot Carrier structure has the greatest dynamic range requirement because we are looking for saturation current changes that are the order of 1 to 10 percent. Fortunately we do not need to accurately know the magnitude of the current in the Hot Carrier test transistors. It is sufficient to know the relative saturation current change from a fresh unstressed device. TDDB measurements need only be fail/not-fail indication and electromigration can be either fail/not-fail (i.e., open circuit/conducting) or relative resistance change. The simplest circuit for digitizing a relative current change is a current controlled oscillator.

The schematic diagram of the Current Controlled Oscillator is shown in Figure 1. It consists of essentially a seven stage ring oscillator with two of the inverter stages modified to have slew rate control via a pass transistor to ground (M16 and M17). The amount of current that the pass transistors can sink is controlled by placing these two transistors in a current mirror configuration (M15, M16, and M17) using M15 as the current input point. Current input through VOSC sets the slew rate of two inverter stages and hence the ring oscillator frequency. It is important to limit the input current to a range that makes the slew rate limited stages act as the

primary ring delay elements. If the input current approaches the nominal saturation current of the unmodified inverter stage the linearity of the current controlled oscillator will suffer.

Simulation results (Figure 2) show a well behaved current-frequency relationship up to an input current of 100μA. At that point the stage delay of the remaining five stages becomes a significant fraction of the delay imposed by the slew rate controlled stages. Over a current range of 0.001μA to 100μA the Current Controlled Oscillator frequency has a power function relationship over that five orders of magnitude of current. The fitted power function was:

$$F = a * I^b \qquad (1)$$ Oscillator Frequency in Hz.

Where a = 4.09694 $X10^5$, b = 0.90522 and I is input current in microamperes. The calculated data is plotted with the simulated data. A correlation coefficient of fit was 0.994. Figure 2 contains a plot of the simulated Current Controlled Oscillator performance compared with this fitted power function.

If we further restrict the operating range to 0.1μA to 10μA the power function fit is quite good with a = 4.48614 $X10^5$, b = 0.8586 resulting in a correlation coefficient of 0.999992. However, since we are primarily looking for small current changes over time of the order of 10%, the transfer function is sufficiently well behaved (and sufficiently close to linear, with $b \approx 1$) to allow operation of the current controlled oscillator over its entire simulated input current range.

Temperature stability of the Current Controlled Oscillator is not relevant in this design application. Clearly there will be a substantial temperature factor in the oscillator frequency at a given input current. Since all self-stressing test structure performance will be compared with unstressed devices or will be assessing a fail/not-fail condition, the temperature dependence of oscillator frequency will not be significant as long as the comparison measurements are made close together in time. This assumes that the test chip is operating at thermal equilibrium.

Frequency measurement is done in the digital control function that will be discussed in a later section. An accurate reference frequency is also not required because only relative changes in current are important.

Layout and simulation results are in Appendix A.

Time Dependent Dielectric Breakdown:

The most challenging design problem for the Time Dependent Dielectric Breakdown (TDDB) test structure is applying enough stress field to the test transistor to enhance the failure rate without stressing anything else on the chip at an accelerated rate. The constraint of having only a

single power supply of 5.0 Volts forces the need to generate a higher potential on chip in such a way that it does not effect any other component on the chip. The additional potential required to stress the oxide was produced by designing a well bias circuit that will pump the well containing the test circuitry to create a larger total potential across the test capacitor. Figure 3 contains the schematic diagram of the TDDB test structure for an N-Well CMOS process. A similar circuit (essentially the dual of Figure 3) can be constructed for a P-Well CMOS process.

The TDDB test circuit in Figure 3 consists of three basic functions: 1) A gated clock buffer consisting of M1, M2, P19 and NR2. 2) Charge pump network consisting of P15, N16, and N17 (which is the gate oxide under stress) 3) The gate oxide failure detector P22. Transistor P15 serves dual function as a charge pump capacitor and a diode connected to the N-Well. N16 is an N-channel transistor connected as a MOS diode.

STRTDDB is the Enable/Disable control, it's logical state is Enable-high, which is latched by CLAT and enables the clock buffer by setting N1 of NR2 to 0.0 Volts. P19 serves as an N-Well isolator (P19 and P22 share the same well, which is isolated from the pumped well) so that the charge pump biased well can be disconnected from the power supply rail during failure testing. Finally, V55 is the pulse clock source which may be almost any frequency of the order of 5.0 MHz or greater. The clock can be derived from an existing ASIC clock source or can be supplied by a ring oscillator contained within the self-stressing test circuitry.

V9 is the failure test indicator. P22 has its gate connected to the pumped N-Well (V4) and is at a potential that is greater than the 5.0 Volt rail. The source of P22 connects to the 5.0 Volt rail and the drain is monitored for changes in current. As long as the test capacitor (N17) has no significant leakage then this transistor will not conduct either because the gate is at a more positive potential than the source or the gate-source potential is zero. If the gate oxide in N17 has a breakdown then V4 will be dragged to a potential that is determined by the threshold of N16 plus a forward diode drop. This will cause P22 to conduct as soon as V4 drops a threshold below the 5.0 Volt rail.

The charge pump circuit transfers charge from the power rail to the well which causes the well potential to increase beyond the rail potential. The clock buffer alternately connects the gate of P15 (used as a capacitor for storing charge) to power rail and ground. When the clock buffer is in the low state the channel of P15 is charged to a voltage one N-channel threshold below power rail through N16, which is a MOS diode.

When the clock driver output is switched to a high state the channel charge on P15 is driven into the well through the source/drain junctions of P15. The charge injected into the well is shared with the gate oxide capacitor formed by N17. As the clock driver switches alternately high and low the potential on the well and the gate of N17 rise. Simulation results show that the well potential (V4) rises to about 6.5 Volts within about 150μs to 200μs. This voltage limit is

determined by the threshold of N16, P15 and the forward junction drop of the source/drain of P15. If P15 and N16 were ideal diodes without forward voltage drop and if P15 were an ideal capacitor without limitations set by channel charge limits it would be possible to achieve a maximum well bias of 5.0 Volts. That would make the theoretical maximum stress bias on the test oxide (N17) 10.0 Volts.

The actual maximum well bias will be determined by the final manufactured threshold of the N-channel and P-channel transistors which can lead to bias voltages ranging from 6.0 Volts to 7.0 Volts. A stress voltage of 6.5 Volts is typical of most CMOS runs through MOSIS. Since 6.5 Volts is 1.3X normal power rail voltage the wear out rate of gate oxides should be significantly greater than at normal potential of 5.0 Volts and should provide useful early warning of lower quality oxides. Oxide failure test results from MOSIS wafer lots using voltage ramp tests at the wafer level show early failures at the range of 6.5 Volts in wafer lots that contained substandard oxide quality.

It should be noted that P15 is also being stressed at elevated potential in this circuit. The stress acceleration is slightly less on the average, but the peak field will also be set by the 6.5 Volt level found on the well. Failure in either gate oxide will be detected.

Test mode is entered by latching a logical low state of STRTDDB into CLAT which disables the clock drive to the clock buffer and also disconnects the source of M1 from the power rail while placing the gate of P15 at ground potential through M2. Removal of M1 source from the power rail eliminates a well discharge path. At this point the charged well is isolated and will slowly discharge through the reverse biased well junction or source drain junctions and the Fowler-Nordheim current in the gate oxide. As long as the well potential is greater than one P-channel threshold below power supply rail P22 will not conduct. If the current through V9 (drain current of P22) is monitored it will be possible to assess the existence of gate oxide that has failed. If the gate oxide of either P15 or N17 has failed the gate of P22 will be pulled toward ground and cause P22 to conduct. Note that there is no way to distinguish between failures in P15 and N17.

The failure ambiguity above can be removed by adding more logic circuitry and adopting a different testing strategy to determine which gate oxide failed by changing states of the clock driver output and testing for leakage to ground again. If only P15 has failed then the leakage path will be eliminated by having the clock driver output at a high state during a failure test. On the other hand if only N17 has failed then the output state of the clock driver will not change the leakage test results. Looking at the layout of the TDDB test structure in Figure 4 it is clear that the majority of the area is dominated by the two capacitor-connected transistors. This refinement was not included in this TDDB structure design to simplify the layout, reduce the area and simplify the testing strategy.

Since there are several normal leakage paths in this circuit the charge condition of the well is a dynamic state when the clock driver is disabled. In order to obtain an accurate assessment of the condition of the gate oxide under test it is necessary to time the testing of the drain current of P22 properly. If the current is monitored too rapidly after disabling the clock driver it may be possible to overlook a gate oxide failure that is high resistance of the order of 500KΩ. On the other hand a long delay may lead to erroneously assigning failure to a test structure. An assumption was made that there will be very few cases where a failed gate oxide will exhibit a leakage resistance greater than about 500KΩ. This was used as a basis for determining the minimum measurement delay for detecting a high resistance oxide failure.

A simulation was run to determine the delay time required between clock disable and V4 decay to the clamp level determined by N16 and the source-drain junction of P15. Figure 5 shows the discharge characteristics and indicates that a delay of the order of 80μs is required to see maximum drain current at P22. A shorter delay of about 50μs is also probably possible if the fail/not-fail current threshold is set to a value in the 50μA to 100μA range. Larger or smaller failure resistance assumptions will lead to proportionally longer or shorter minimum delay times for a given clamp level.

Having set the lower delay bound above, the determination of the upper bound of delay is more difficult. It is not possible to accurately simulate junction leakage current or Fowler-Nordheim current with SPICE. However, it would not be unreasonable to set the upper bound to be at least 10 times the lower bound. Maximum measurement delay of the order of 1.0ms is not an unreasonable demand to place upon the boundary scan controller. It is a simple matter to string a clock disable command and a measure command separated by between 80μs and 1.0ms.

Layout and simulation results are located in Appendix B.

Hot Carrier Damage:

The hot carrier damage self-stressing test structure was intended to be capable of detecting changes in channel mobility of the order of less than 1%. A differential amplifier design that had one transistor of the pair placed under stress bias while the second transistor was subjected to little or no stress. Small changes in mobility would show up as a change in differential drain current which would be amplified by the gain of the differential pair. This circuit depended heavily upon a voltage mode A/D converter which turned out to be impossible given the design constraints we had set. A different approach was developed that depends upon the ability to see small changes in drain current directly.

The hot carrier damage self stressing circuit is shown in Figure 6, which is an extracted schematic from the geometry file. Test transistors are indicated as N49, N51, N63 and N64 and

are interdigitated pairs of transistors. Interdigitated layout is used in all parts of this design where it is desirable to have good matched characteristics between the stressed transistor and the unstressed transistor and their respective current monitoring circuits. N48 and N63 make up the stressed transistor while N51 and N64 make up the unstressed transistor. A similar interdigitated structure is used for the current mirrors that are used for the current measuring circuits. P44, P45, P66 and P67 form the current mirror for the stressed transistor. P46, P47, P68, and P69 form the current mirror for the unstressed transistor.

Gates of the two test transistors are connected to a bias source that places the gates at a voltage that will cause the most rapid hot carrier degradation at 5.0 Volts on the drain. The bias circuit is simply a well resistor connected between power rail and ground that is tapped at the appropriate point. Sources of each of these transistors connect to the drain of a disconnect transistor (N49, for the stressed transistor, and N50 for the unstressed transistor) that provides the means for interrupting current flow. Finally, P65 is used to bypass the current mirror in the drain of the stressed transistor during the stress cycles by placing V11 at ground.

Stress bias is applied to the test transistor by setting V9 at power rail (5.0 Volts) and V11 at ground. That places the drain of the test transistor at 5.0 Volts and the source at ground. The bias network tap (V6) is set to apply slightly more than twice transistor threshold voltage to the gate. Under these conditions the test transistor is subjected to the greatest hot carrier damage rate for a 5.0 Volt power supply. While the test transistor is under stress bias the reference transistor is disconnected by placing V10 at ground. This prevents any hot carrier aging from occurring in the reference transistor during stress intervals. Stress current can be removed from the test transistor by simply connecting V9 at ground potential.

Measurement of changes in drain current caused by hot carrier damage is accomplished by setting control ports V11 to ground, V9 and V10 to power rail (5.0 Volts). V6 remains set to the stress gate bias because it does not really matter what the gate bias is for measurement of drain current changes as long as the gate bias is greater than threshold. Current measurements are made by alternately connecting V5 and V4 to the current controlled oscillator.

Even though some effort was made to produce identical transistors for the test transistor and the reference transistor it must be recognized that there will be some differences between them. Both transistors must be exposed to identical amounts of measurement stress current, even though the hot carrier damage rate under measurement bias is very small. It is also very important to make current reference current measurements on both transistors before stress current is applied to the test transistor for any significant amount of time. In order to compensate for the possible existence of mobile ions the gate bias, V6, remains applied to the reference transistor during the stress cycles on the test transistor. Any threshold changes that may be caused by mobile ions will effect both transistors in the same way.

Simulations of this hot carrier test circuit were obtained by extracting sets of SPICE model parameters from measurements on both hot carrier stressed and unstressed N-channel transistors. Hot carrier stressed SPICE parameters were obtained by stressing a 2.0μm channel length transistor (the geometry used in the test chip design) with a drain voltage of 7.0 Volts and with a gate bias that maximized the substrate current. I/V measurements for model parameter extraction were made before stressing and after 100 sec., 1000 sec. and 10000 sec. of stress time at the above bias conditions. These parameters were used to compare drain current of the reference transistor with the drain current of the test transistor. Figures 7, 8, 9, and 10 show these results. Note in Figure 8 the drain current change after 100 seconds of stress was about 2% (I_T/I_R=0.981). If we apply Equation 1 with the drain current of both transistors we will see that there will be approximately a 2% change in frequency (F_T/F_R=0.983) of the current controlled oscillator. For the current levels simulated the current controlled oscillator has an output frequency of approximately 13 MHz. Since the frequency counter register is 16 bits it will easily be possible to measure a frequency change of 2%. Greater than 10% current change is observed after 10000 seconds of stressing, which is as long as the stress testing was conducted.

It is clear that since we are only concerned about relative changes in performance then we should be able to resolve 1% differences in current based upon the simulation results. Also, it is clear that since the maximum drain voltage that can be used in stress mode is 5.0 Volts the stress times to achieve 10% current change will be long. Aging data on transistors with 5.0 Volt drain bias have not been made, but measurements made at 5.5 Volts indicate that the aging rate is about 1/150 times the rate at a drain voltage of 6.5 Volts. However, since the gate bias is chosen to maximize the hot carrier degradation rate this test structure should be a suitable moderate acceleration test for digital circuits.

Layout and simulation results are located in Appendix C.

Electromigration:

A self-exercising electromigration test structure is the most difficult to realize compared with the previous two cell designs. In order to apply even a modest amount of stress to interconnect metal it is necessary to supply current in the order of 10.0mA. Even this amount of current may be excessive in a low power ASIC application. Since the level of current that is required for each test line is large, and since the total power supply voltage is 5.0 Volts, there are significant design constraints imposed on a self-exercising electromigration test structure. Furthermore the requirement that only low current measurements could be used for failure assessment restricts the type of failure detection that can be made. The design that was chosen is only one of several that could have been implemented.

In developing the cells for the selected design there was consideration given to the area occupied by the cells. Version 1 was designed to be a minimum area test structure while sacrificing stress

current regulation and the ability to approximately measure relative resistance changes in the metal test line. Version 2 was implemented to provide relative resistance change measurement and stress current regulation. Version 2 cells occupy significantly larger area on the silicon.

The Version 1 self-exercising electromigration test structure is comprised of three parts: 1) The metal resistor string. 2) The failure detector multiplexer. 3) Test Control Logic. This test structure is the largest area test structure of the three mechanisms because the test resistor consists of very long meanders in order to have a total resistance of the order of 500Ω. A 500Ω resistor string serves as the stress current limiter in the test. 500Ω was chosen because we arbitrarily set 10mA as the maximum stress current for the test structure, which corresponds to a current density of about 4 $X10^5$ A/cm^2 in metal 1 and 3.3 $X10^5$ A/cm^2 in metal 2. These current densities result from design rule constraints on minimum line width (also metal deposition thickness) for the fabrication process that was used for the test chip. For other fabrication lines with finer feature sizes this stress current density will increase proportional to the design rule width limits. Given that most CMOS fabricators specify design limit current density of ≤ 1 $X10^5$ A/cm^2, these current densities correspond to moderately accelerated stress testing and will serve as an adequate metal lifetime monitor.

The resistor string consists of eight segments of meanders (Figure 11, schematic and Figure 12, layout), each with a resistance of approximately 62Ω and with different metal layers and topographies. The segments are: 1) Metal 2 on flat oxide. 2) Metal 2 over metal 1 steps. 3) Metal 2 to metal 1 via string. 4) Metal 1 over flat oxide. 5) Metal 1 over polysilicon steps. 6) Metal 1 over active area steps. 7) Metal 1 with contacts to polysilicon. 8) Metal 1 with contacts to active area. There are no contact strings in this test structure because there is experimental evidence that contact electromigration is many orders of magnitude less failure rate than the interconnect metal. The top end of the metal 1 meander is connected to the power rail and the bottom end of the metal 1 over contacts to active area is connected to a large N-channel transistor (about 1000μm wide and minimum channel length) that acts as a stress current switch for the metal resistor string and has a voltage drop of less than 0.2 Volts at 10 mA. Connecting links between segments of the resistor string are monitor taps. These links use layout geometry that is sufficiently robust that there is very low probability that they will be a failure point under the stress current selected.

All metal runs in the meanders are minimum design rule width to save area in the resistor string. There is a case for using metal widths of at least twice minimum design rule width because a minimum width metal run may be a bamboo structure which would not reflect the worst case metal failure rate in a chip. We selected the minimum geometry case to keep the test structure area as small as possible. Increasing the metal width by a factor of two will increase the resistor string area by about a factor of four and will increase stress current requirements by a factor of

two. Since the minimum structure is rather large, we decided not to include the large metal width case in this cell set.

The failure detector multiplexer is another compromise in design to limit chip area. This circuit is shown in Figure 13 and includes a P-channel multiplexer (P44 - P51) along with a test current source and complementary current mirror (R85, N76, N77, P74, and P75) that is used to detect open circuit failures in the resistor string. Transistors P52 - P58 are used to provide a current path to power rail so that multiple resistor opens can be detected. It functions by using the resistor segment under test as a path to power rail, which causes current from N76 to be shunted to power rail and causing P75 to be cut off. A failure is detected when the shunt current path to power rail is open and allows current from N76 to be reflected through N74 to N75 and thence to the current controlled oscillator through the system test multiplexer. Test current is limited to 0.1 μA to avoid exceeding the useful range of the current controlled oscillator. Current this low does not permit measurement of resistance in the resistor string. This is a serious limitation in applicability when interconnect metal systems contain refractory layers to reduce the chance of open failures caused by electromigration.

Figure 14 is the schematic diagram of the multiplexer address latch and decoder. This circuit is used to enable testing (ENB) and to select the resistor segment to be tested for open failure. It is simply constructed with CMOSN cells. Inputs to the latches come directly from the boundary scan cells.

Electromigration (Version 2):

Having defined the minimum self-exercising electromigration test structure, we will now look at some simple revisions to this design to improve stress current regulation and to allow monitoring individual resistor segments for resistance changes. The goal for resistance changes is to be able to detect a 10% resistance increase and report it as a failure. It is common in the semiconductor industry to define a 10% resistance increase as an electromigration failure in composite metal systems. The revised test structure will still use minimum width metal runs to keep the area minimized and to keep the stress current level at about 10 mA.

The first revision to the above design is to provide a somewhat more stable stress current control. This is accomplished by using a simple ratioed current mirror to set the stress current, and for that matter the test current, on the resistor string. By using roughly a 10:1 ratio of transistor sizes in the current mirror it is possible to reduce the reference current by a factor of ten. The reference current is derived from a well resistor and is subject to considerable variability in fabrication (± 20%). However, since the absolute value of stress current is easily determined by measurement after fabrication it is not important that the reference resistor has a tolerance of ±20%. This tolerance will not effect our ability to detect a 10% change in metal resistance because we are always making relative resistance measurements and the absolute

value of current is unimportant as long as the current is sufficiently stable over time. Any time dependent measurement current changes can be removed by simply measuring the test current at the chip level by observing the supply current changes that occur with the electromigration stress/measurement current source enabled and disabled ($I_{EM} = I_{ENB} - I_{DIS}$).

Revision of the resistor chain is driven primarily by the need to keep the metal runs as long as possible while keeping the total chain resistance below about 250Ω to prevent the current mirror from operating in the transition region between linear and saturation. Long metal runs are desirable to increase the number of vacancies that can coalesce to form a void in the metal run and to have a sufficiently large resistance to be able to easily detect a 10% resistance change. A segment resistance of 31Ω was determined by simulation to be a good compromise between total maximum resistance and the resistance change resolution. With this change the resistor chain area is decreased by about a factor of two.

The Version 2 multiplexer in Figure 15 has changes in order to be able to place each resistor segment to be measured at a potential near power rail. This strategy is necessary to place the current controlled oscillator in an operating region where it is most linear and able to resolve small changes in resistance. The pull-up transistors described earlier (P52 - P58 of Figure 13) must be made wide enough to present a saturation resistance that is much smaller than the 31Ω resistor segment. Simulations indicate that the width of these transistors must be increased to 2000μm (P40-P43, P59-P61), which has a serious implication in test structure area. The 7 transistor set area has become larger than the resistor array area. In addition, the multiplexer transistors (P44 - P51 of Figure 13) must be augmented in order to provide a simple measurement access to each resistor segment such that the voltage at both ends of the resistor segment can be measured. Figure 15 shows a schematic diagram of the revised measurement circuit with the dual rail measurement bus. Transistors P76, P79, P81, P83, P85, P87, P89, P126 connect the high end of each metal resistor to the High Rail, and transistors P77, P78, P80, P82, P84, P86, P88, P127 connect the low end of each metal resistor to the Low Rail. The final measurement multiplexing is done with P128 and P106 to connect the High Rail and the Low Rail respectively to the measurement circuit. The measurement circuit consists of a long well resistor with a total resistance of about 100KΩ to convert the voltage levels to a current that can be sensed by the current controlled oscillator. The large resistance is required because the voltages being measured are near the power bus potential (5.0 Volts) and because the maximum useful linear operating region of the current controlled oscillator is in the tens of microamperes.

The stress current source (or more correctly the current sink because the resistors are connected to the power bus) now serves a dual function. It must be both the stress current source and the measurement current source. A scaled current mirror is implemented with transistors N117, and N119 with a well resistor (about 2500Ω) connected to the power bus to supply the reference current. This reference current is set to about 1.0 mA and the current mirror scale factor is about

10 so that the stress current is about 10 mA. Transistor N130 provides a path to shunt the reference current to ground to disable the stress/measurement current.

The dual measurement rail is alternately sampled using a two input multiplexer (P128, P106) to get $V_{High} - V_{Low}$ from each resistor segment while the high end of the desired resistor segment is held near power bus potential by one of the large pull-up transistors. The change in potential difference across the resistor segment being tested results in a change in current controlled oscillator frequency differences ($F_{High} - F_{Low}$) which will provide the basis for determining a relative segment resistance change. This relative resistance change is represented by:

$$\frac{\left(\left(F_{High} - F_{Low}\right)_{t2} - \left(F_{High} - F_{Low}\right)_{t1}\right)}{\left(F_{High} - F_{Low}\right)_{t1}} \propto \Delta R\%$$

where the subscript t1 is the measurement made at the beginning of the stress period and the subscript t2 is a measurement made at a later time. When ΔR% is greater than 10% the resistor segment is considered failed due to electromigration caused voiding.

Figure 16 is the schematic diagram of the revised multiplexer address latch and decoder. As with Figure 14 this circuit is used to enable testing (ENB) and to select the resistor segment to be tested for resistance change. An additional pair of states is added as one latch and two NAND gates to select the High Measurement bus (H_) or the Low Measurement bus (L_). It is also constructed with CMOSN cells. Inputs to the latches come directly from the boundary scan cells.

Layout and simulation results for both the basic and revised electromigration test structure designs are located in Appendix D.

Boundary Scan Interface and Test Structure Controller:

The boundary scan example given here is a very simple structure that is intended only for a rudimentary demonstration of the self-stressing test structure capability. There are no sophisticated decoded instructions or internal timing generators. All timing functions for the controller are derived from the boundary scan clock. This greatly simplifies the demonstration of the test structure library and assumes that the test chip will be tested in a test system that is totally dedicated to testing the self-stressing test structures. A more sophisticated controller would only remove the timing burden from the test hardware and would not produce a more accurate set of data. Initially, all of the cells from this self-stressing cell library would have been fabricated in a test chip, but because of some design rule compatibility problems in the first (unsuccessful) test chip, the controller logic described here is what the second test chip would have used.

Basic functions that the controller must perform include: 1) Enable/Disable Stress bias conditions on the test structures. Note that the stress factor is generally fixed for these self-exercising test structures. 2) Provide measurement access addresses where multiple structures are used. 3) Provide frequency measurement circuitry to convert current controlled oscillator output to a digital quantity for data logging. 4) Provide a clock source for self-exercising structures that require a clock.

The primary function performed by the controller is to supply control signals for current controlled oscillator frequency measurement. The GATE signal is used to connect the current controlled oscillator output to a 16-bit counter for frequency measurement. Duration of GATE is set such that the highest expected frequency from the Current Controlled Oscillator will not overflow the 16-bit counter. The controller also generates a counter reset (RST) after the count contained in the 16-bit register data has been stored in the boundary scan output data register (DS).

For control purposes, signals are generated to store measurement address (AS, Address Strobe, such as for electromigration resistor failure testing) and State Strobe (SS), which sets or disables stress conditions in test structures. These signals are only strobe functions. The actual Address or State values are supplied from the boundary scan registers at the time that these signals are generated.

All of the above control functions are generated in a Finite State Machine (FSM) shown in Figure 17. Inputs to the FSM are CLKA and CLKB, which are obtained from the boundary scan clock bus. CLKB serves to mark the time when the data from the self-exercising test structures is collected and when new states for the self-exercising test structures are installed. The FSM supplies the GATE timing for the current controlled oscillator frequency measurement. The FSM design shown here assumes a 10 MHz CLKA frequency. If some other GATE function reference frequency is used, then it may be necessary to modify the modules of the GATE counter. Simulation results of this FSM timing function are included in Appendix E.

In an application where the self-stressing test structures are placed in an ASIC to monitor critical wear-out parameters the specific boundary scan architecture for the test structures would be determined by the boundary scan architecture of the entire ASIC, and even by the overall system architecture in which the ASIC will be used. Since the minimized boundary scan function that was designed for the self-stressing structure test chip depends upon one of the boundary scan clocks to supply a clocking function for the TDDB well bias circuit it will be necessary to obtain that steady state clock function from some other source if the boundary scan architecture in the host system does not supply boundary scan clocks at all times. This should present no problem for the designer because there will usually be a system clock in the ASIC that will serve this purpose. The frequency of the substrate bias clock is not critical as long as its frequency is

greater than 5MHz and less than 50MHz. If access to the ASIC system clock is not practical, then it is only necessary to include a ring oscillator in that frequency range in the self-stressing test structure boundary scan control function.

Discussion and Recommendations for Future Work

The test structures included in this report were designed for implementing a basic self-exercising reliability monitoring capability for package level reliability testing. They allow extension of reliability testing from wafer level to package level imbedded within an ASIC device. They also allow construction of a package qualification reliability test chip that incorporates a simple boundary scan access to all test structures during a test either inside an environmental chamber or any other test environment.

A moderate size test chip can be implemented to conveniently study moderate acceleration factor reliability testing in electromigration, hot carrier damage, and time dependent dielectric breakdown. These chips would be placed in a test board and linked together through the boundary scan interfaces to allow simple monitoring of the test by a small personal computer. A system of this type could be used to approximately model the reliability characteristics of a complex ASIC-based system in whatever environment is appropriate. The test chip cost would be relatively small and the board level array could represent a fairly complex system.

The main disadvantage of these self-exercising test cells is that they are designed for operation under DC stress conditions. Even though the DC stress test results are valuable, it is highly desirable to have a companion set of self-exercising test cells that permit pulsed DC and AC stress testing. In addition, it would be desirable to increase the stress levels selectively so that higher acceleration factors are possible. It would be desirable to relax the 5.0 Volt restriction and the single power supply restriction in cases where the self-exercising cells are being assembled into a dedicated reliability test chip for package or MCM substrate qualification. Relaxing these restrictions would shorten times for accumulating statistically significant numbers of failures.

Pulsed DC stressed versions of the self-exercising cells contained in this report would be relatively simple. However, construction of AC stressed versions will be more challenging and may require dual power supplies and incorporation of external components to make the implementation simple. In any case it is important that the new self-stressing test structures with pulsed DC and AC stressing capability be implemented in a way that emulates stress conditions that actually occur in various circuit applications within ASIC devices.

Future work should concentrate upon improving the accuracy and stability of the measurement circuits in the self-stressing cell library. In addition the effort must extend the cell library to include pulsed DC and AC stressed cells along with means for increasing the acceleration factor beyond the restrictions imposed upon the cells developed under the task reported here.

Electromigration structure cells can be easily extended to include wider metal meanders and stress current sources that have binary programmable stress current level. The higher stress current structures will be, to some extent, self heated when included in a test chip that is dedicated to electromigration. A chip temperature monitor would need to be included in the cell library to enable chip temperature monitoring in order to calculate the correct stress factor. It is also relatively simple to extend these new structures to include pulsed DC and AC stressing.

For the Hot Carrier test structure a revised version should include pulsed DC and AC stressing along with the capability to test the stressed transistor in both directions of conduction. On-chip pulsed DC and AC hot carrier test structures are more likely to be devoid of the problems that come with impedance matching errors that can result in uncontrolled stress factors caused by transmission line reflections and ringing. Even so, a great deal of attention must be paid to proper power and ground routing and off-chip interfacing to prevent ground/power bounce, which would corrupt the control of stress factor on-chip.

Finally any new work should incorporate these new self-stressing test cells along with the current self-stressing cells into a package qualification test chip. This chip should include test structures similar to those which were developed at Sandia for package level testing. Structures such as the thermal conductivity structures and the die stress measurement structures are especially desirable. A combination package qualification test chip would be a very powerful tool for use in linking the wafer fabrication reliability testing with the package level reliability effects to allow an integrated view of reliability limiting factors in ASIC applications.

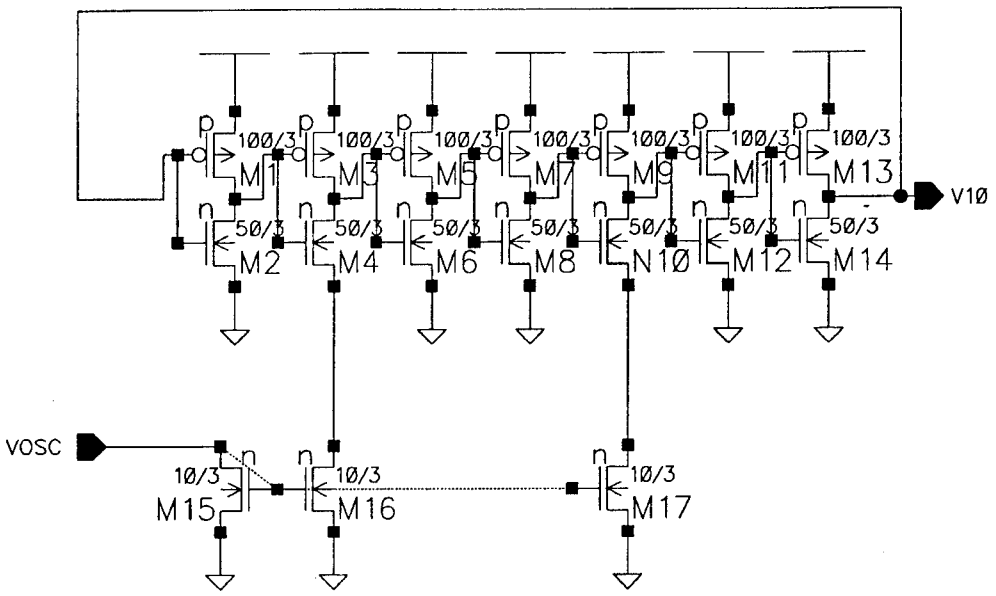


Figure 1: Current Controlled Oscillator - A simple current controlled oscillator is implemented using a ring oscillator with current controlled slew rate.

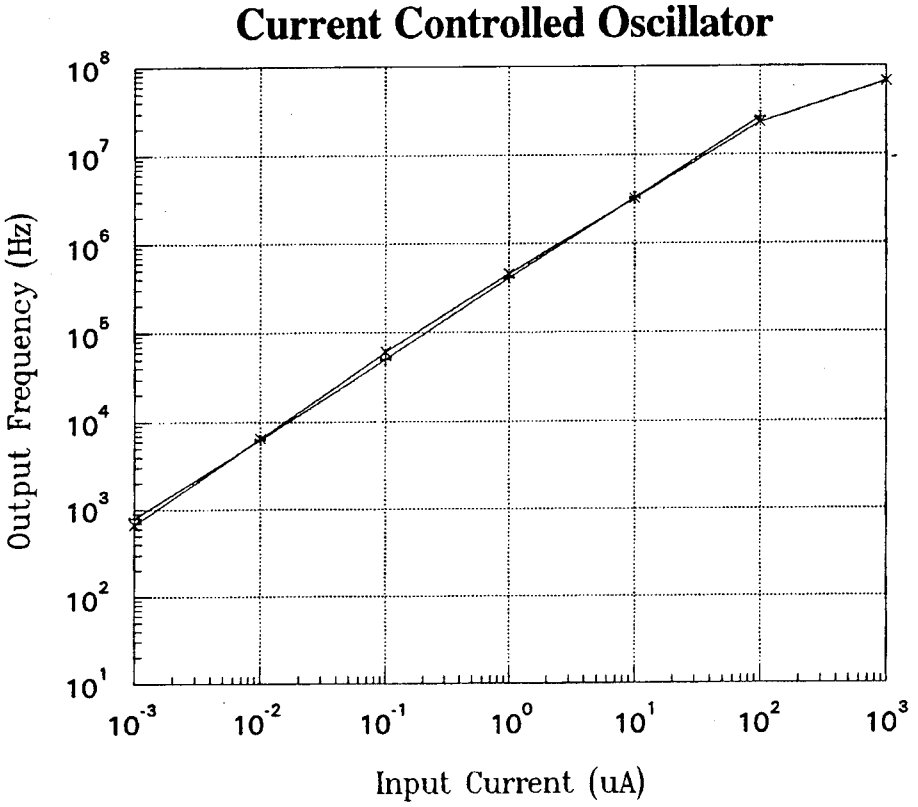


Figure 2: Plot of frequency vs. input current from current controlled oscillator SPICE simulations. (× = Simulation Results; + = Model Fitting)

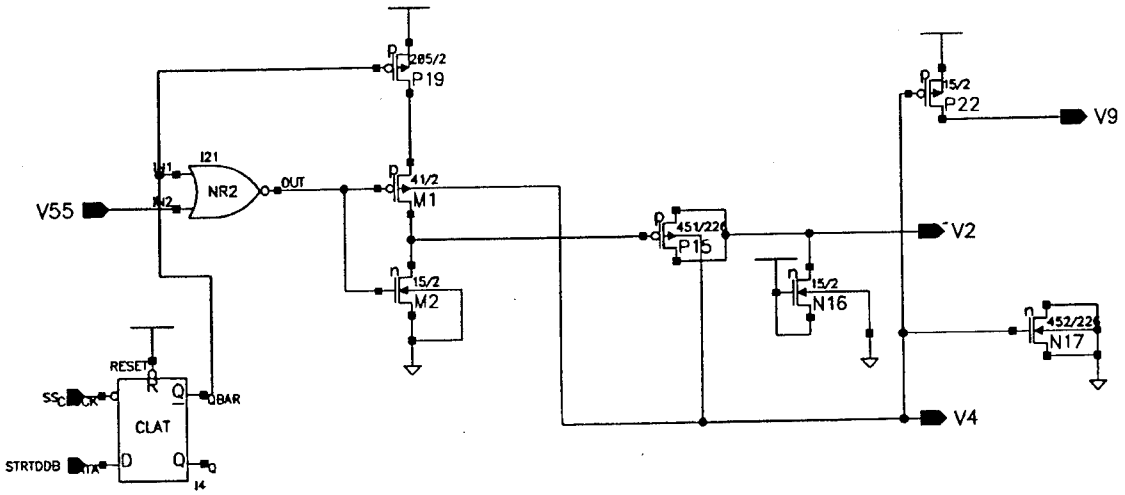


Figure 3: Self-stressing TDDB Test Cell - A well bias generator supplies additional stress bias for increased field acceleration factor.

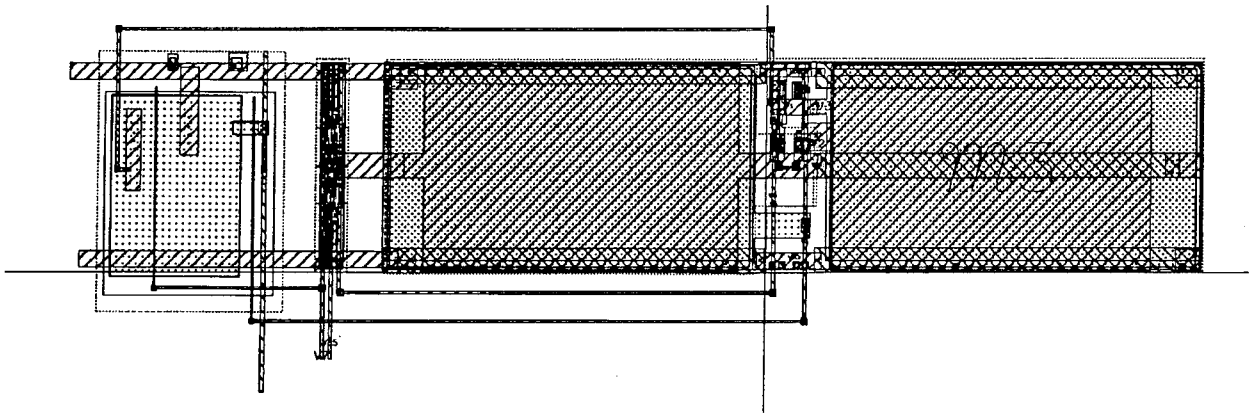


Figure 4: Layout of the TDDB Test Cell - The area is dominated by gate oxide capacitors.

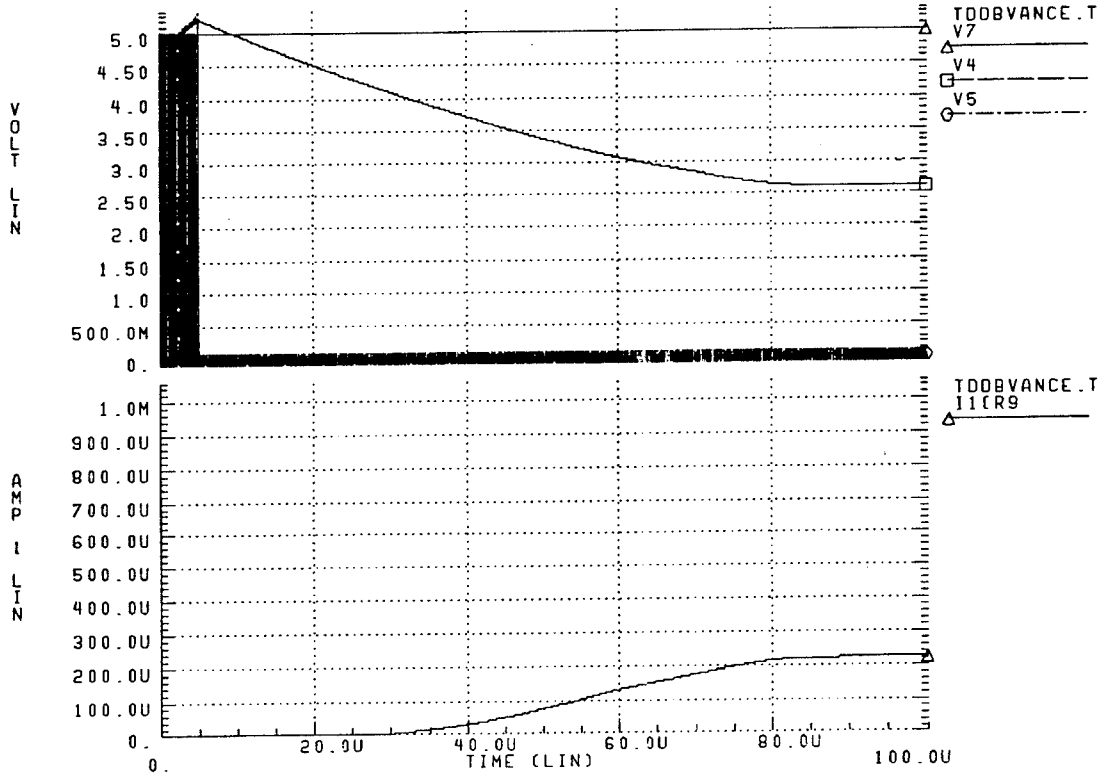


Figure 5: Leaky Capacitor Simulation - The TDDB cell simulation includes a 500KΩ leakage path around the test capacitor. The graph shows the decay time to fault detection threshold.

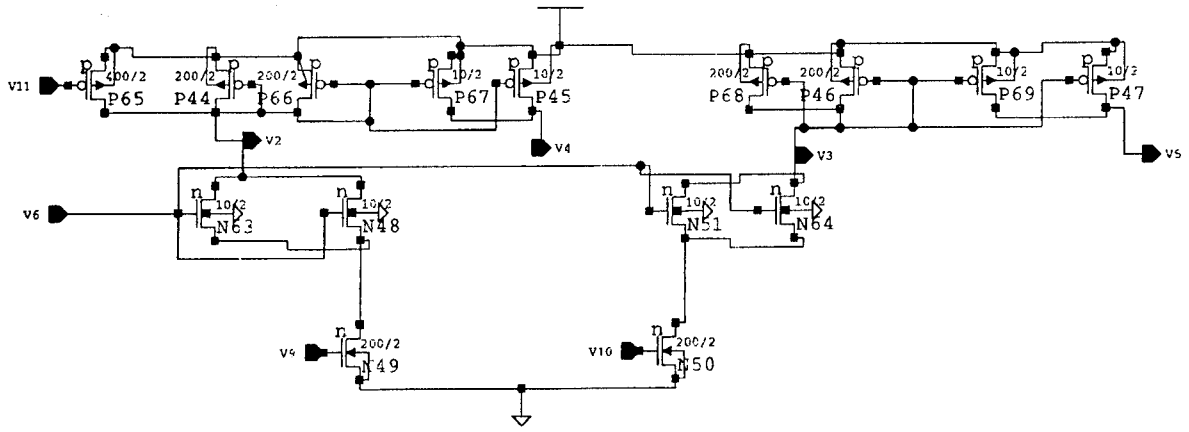


Figure 6: Self-stressing Hot Carrier Damage Cell Schematic Diagram - The circuit extracted schematic shows parallel connected transistors indicating the presence of the common centroid layout.

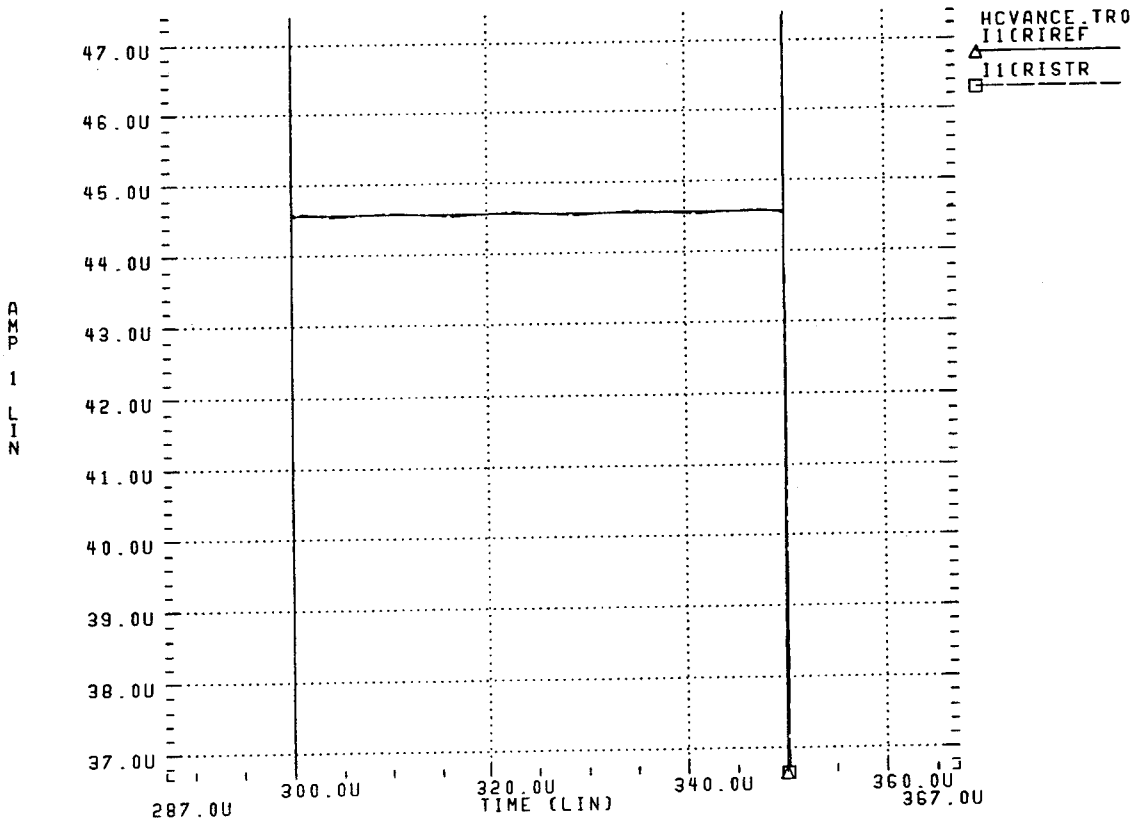


Figure 7: Hot Carrier Damage Cell Simulation - Before hot carrier stress.

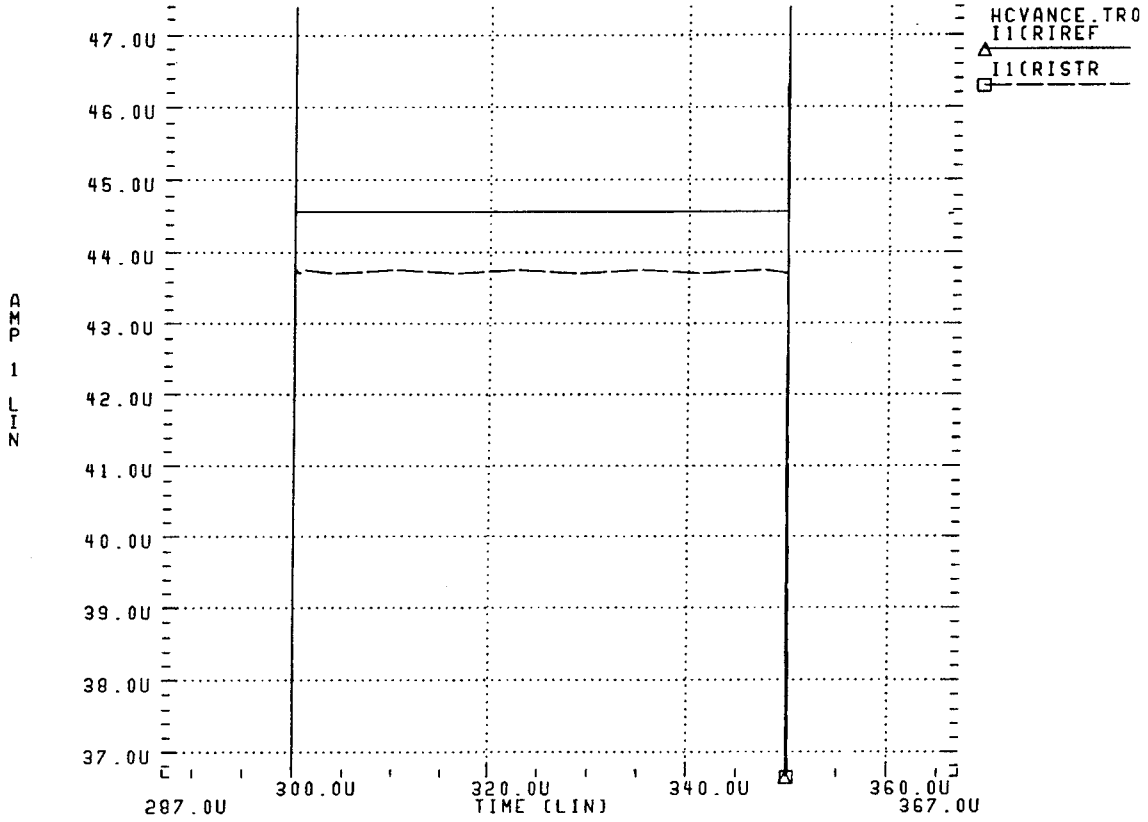


Figure 8: Hot carrier Damage Cell Simulation - After hot carrier stress at Vdd = 7.0 V., Vgs = 2.1 V. for 100 seconds. Note slightly less than 2% drop in saturation current in the stressed transistor compared with the unstressed device.

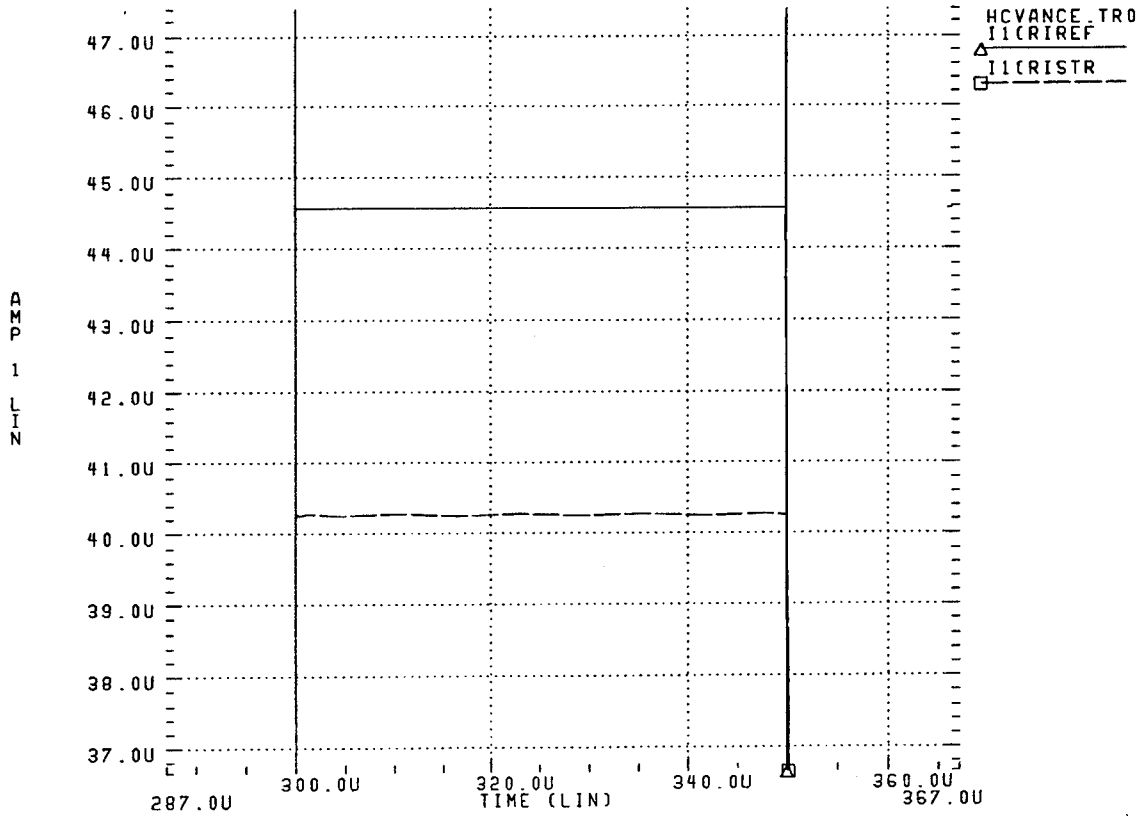


Figure 9: Hot carrier Damage Cell Simulation - After hot carrier stress at Vdd = 7.0 V., Vgs = 2.1 V. for 1000 seconds. Note slightly less than 10% drop in saturation current in the stressed transistor compared with the unstressed device.

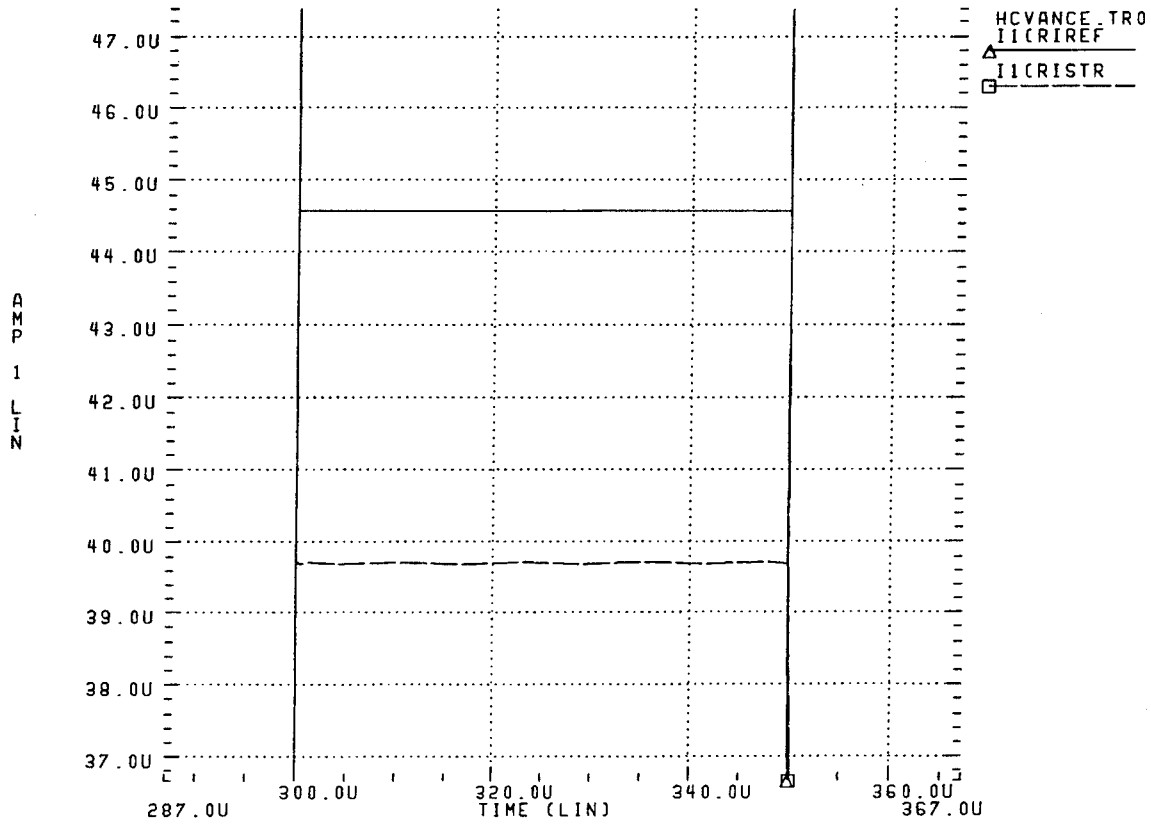


Figure 10: Hot carrier Damage Cell Simulation - After hot carrier stress at Vdd = 7.0 V., Vgs = 2.1 V. for 10,000 seconds. Note slightly more than 10% drop in saturation current in the stressed transistor compared with the unstressed device.

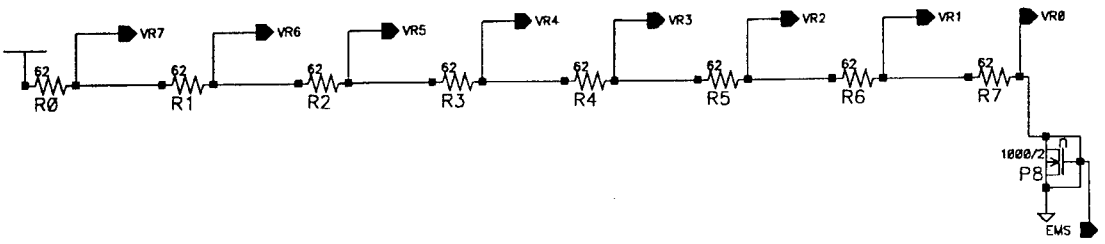


Figure 11: Version 1 Metal Resistor String Schematic - Includes the stress current switch transistor. Current is limited by the total resistor string resistance at Vdd = 5.0 Volts.

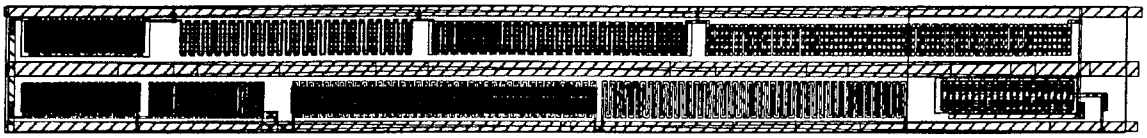


Figure 12: Version 1 Metal Resistor String Layout - A large area structure compared with other self-stressing cells.

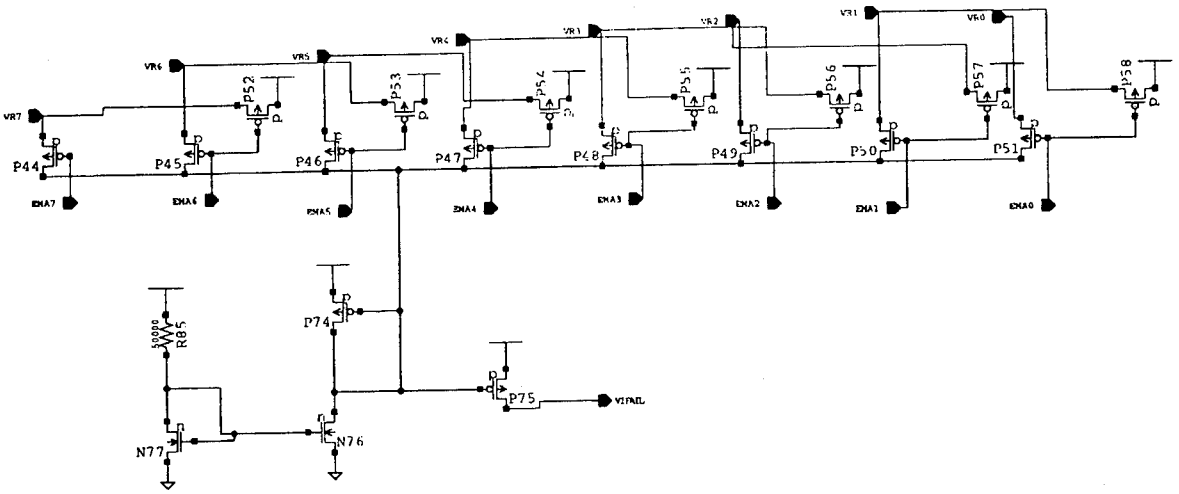


Figure 13: Version 1 Failure Detector Multiplexer - Only open circuit metal line failures are detectable with this circuit.

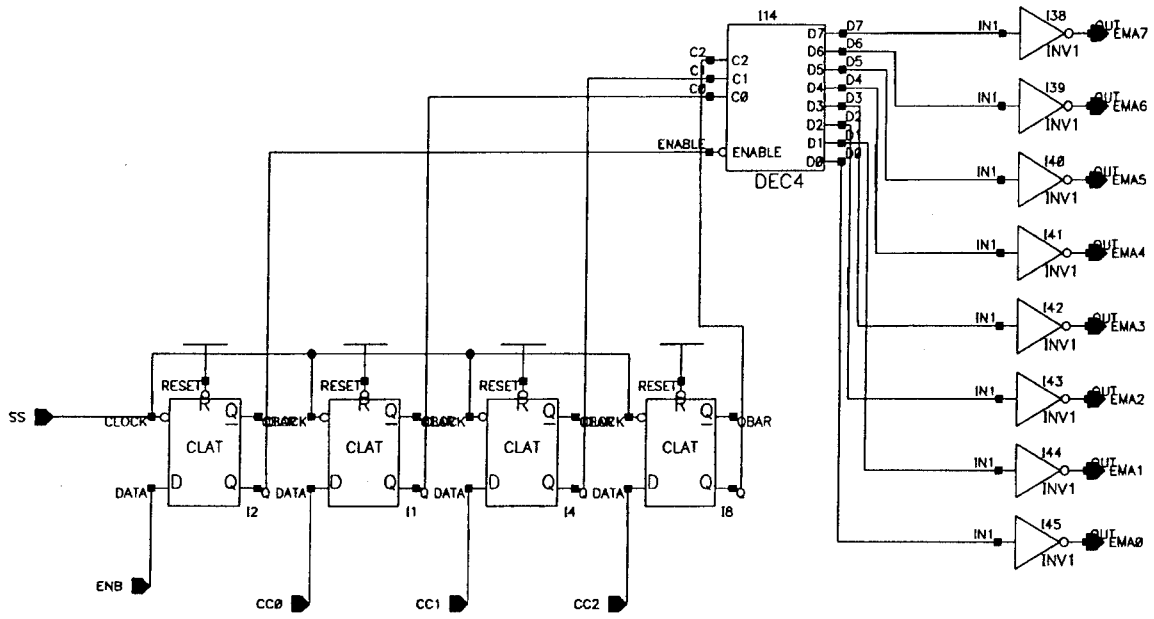


Figure 14: Version 1 Multiplexer Address Latch and Decoder Logic Diagram.

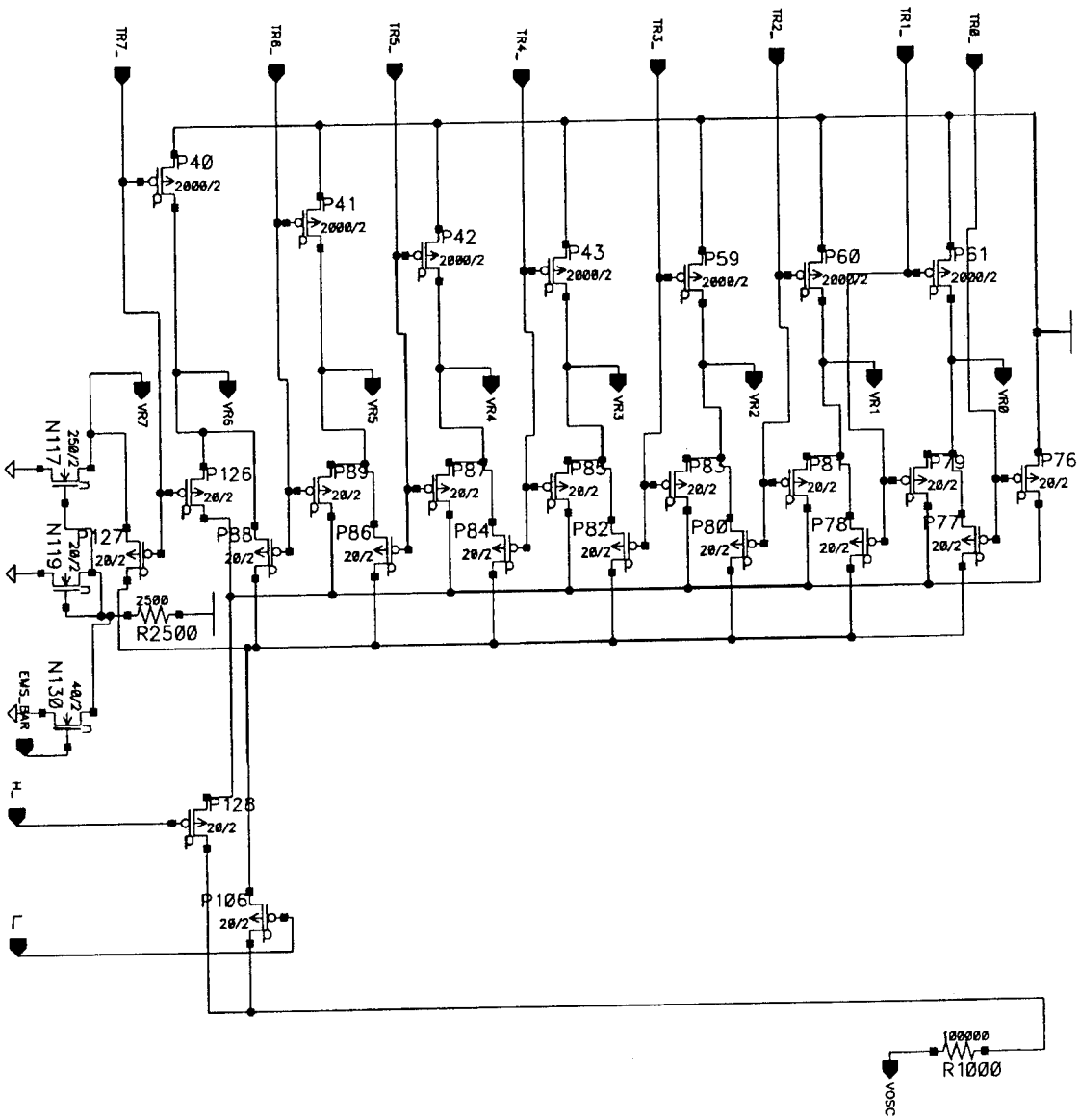


Figure 15: Version 2 Failure Detector Multiplexer - Large resistor segment bypass transistors place resistor segments that are to be measured near the Vdd rail potential in order to allow simple voltage to current conversion with a 100KΩ well resistor. Also, note that the stress current is limited by a current mirror which doubles as a test current regulator.

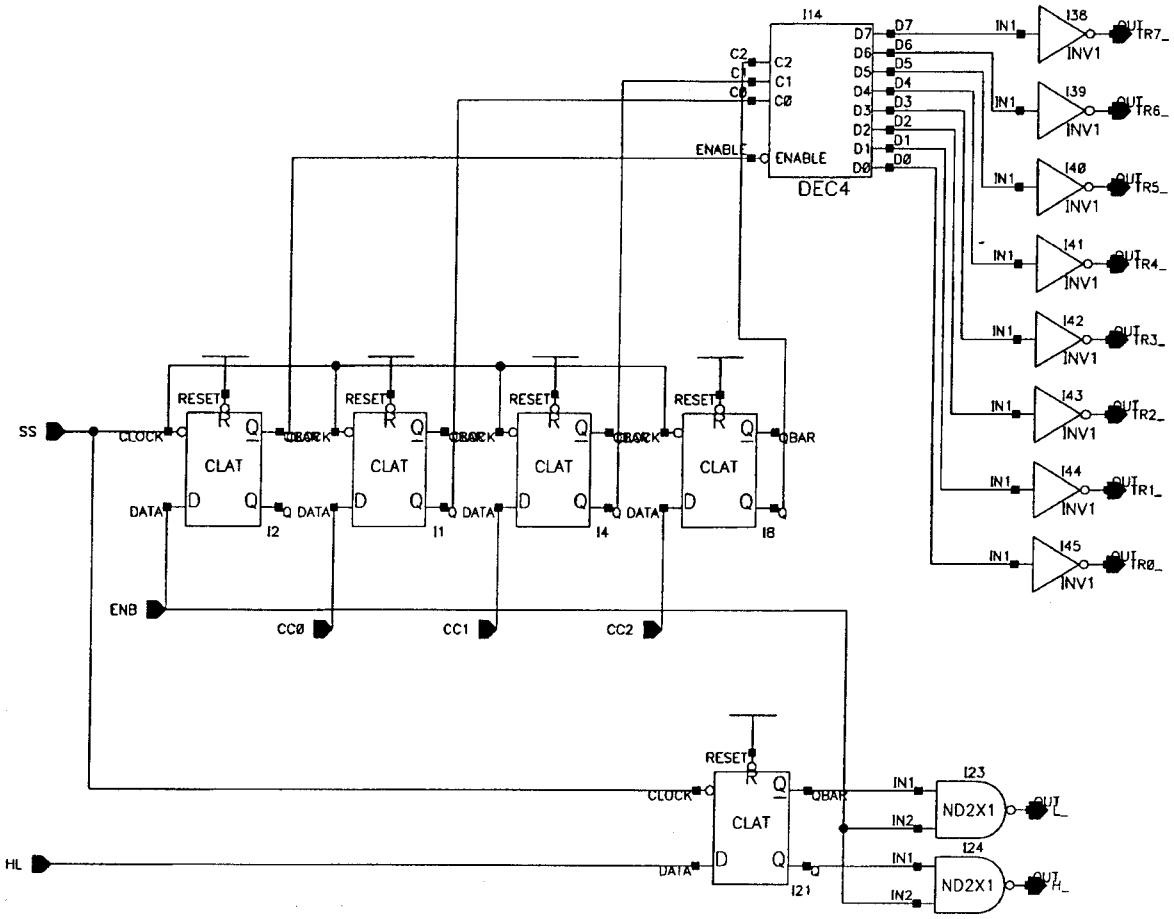


Figure 16: Version 2 Multiplexer Address Latch and Decoder Logic Diagram - Requires only an additional flip-flop plus two NAND gates compared to Version 1.

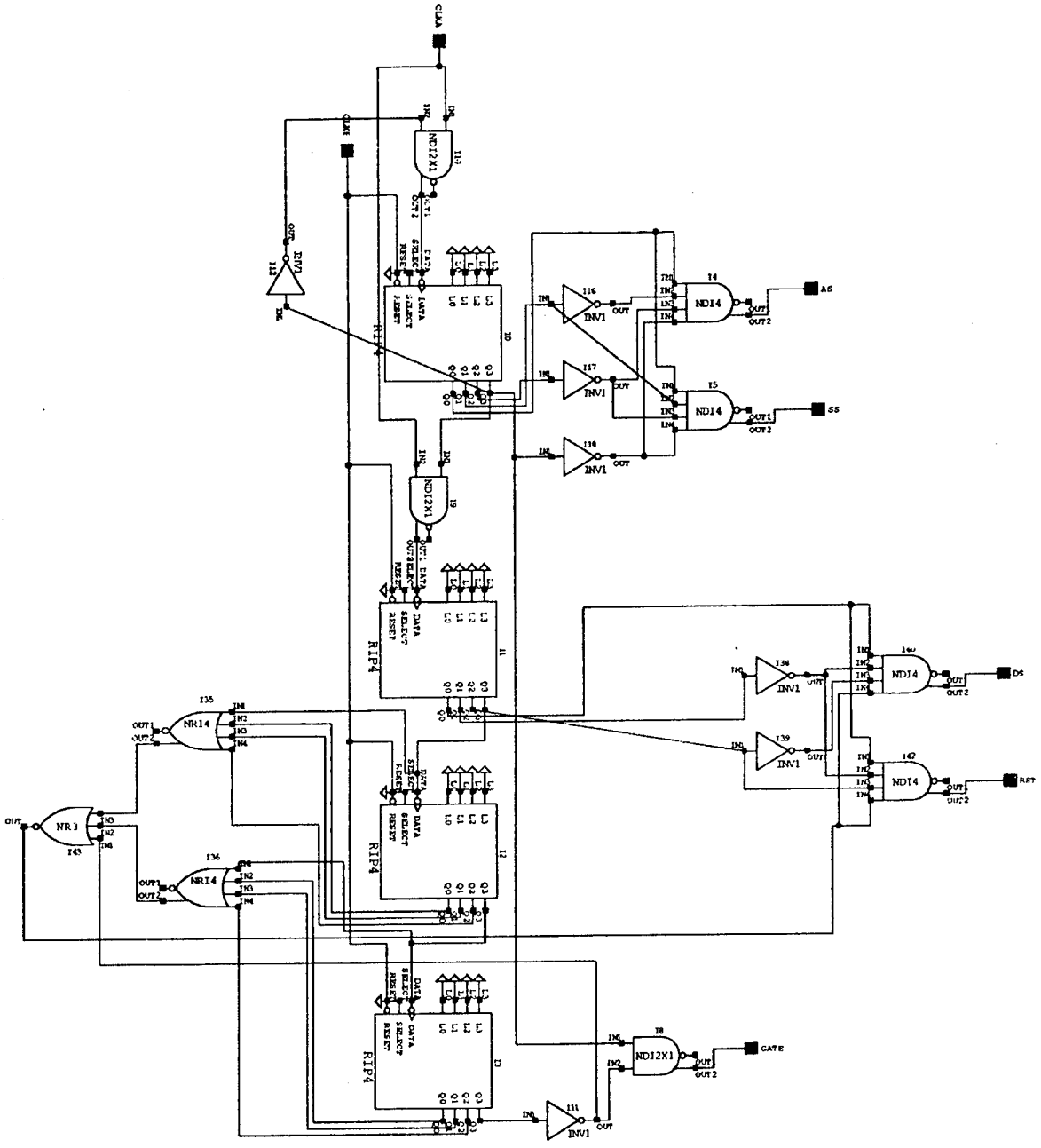


Figure 17: Test Structure Controller - The Finite State Machine provides control signals to enable measurement of current controlled oscillator frequency.

Appendix A

Current Controlled Oscillator Cell

Current Controlled Oscillator Cell

This appendix contains the details of the simulations and the layout of the Current Controlled Oscillator Cell. Simulation results are shown graphically to illustrate the output wave from the current controlled oscillator. The frequency vs. input current information is derived from the period of the waveform from the simulations. There are slight errors in determining the period from the graphical output, but there is enough accuracy to determine when the current controlled oscillator deviates from a simple power law curve fit.

Figure A1 is the schematic diagram of the oscillator and Figure A2 is the layout of the cell. The simulations spanned a range of 0.001μA to 1000μA to fully explore the working range of this circuit. The seven plots, Figures A3a - A3g show the results of SPICE simulations that serve as the basis for extraction of the Current Controlled Oscillator transfer function. The three plots that follow (figures A4a - A4c) the output results are of frequency vs. input current with three different ranges of current to which a power function was fit.

The first plot (Figure A4a) shows the fit for the entire tested input current range. Fitting results give a value of a = 347080 and b = 0.851 with a correlation coefficient of 0.996. The fit is not bad, but there is clear evidence of saturation above 100μA.

The second plot (Figure A4b) shows the fit for the input current range of 0.001μA to 100μA. Fitting results have improved significantly with a = 409694 and b = 0.905 with a correlation coefficient of 0.9994. This is a reasonably acceptable fit given that we are only interested in relative changes of current from the measured self-exercising test structures.

Finally, the third plot (Figure A4c) restricts the operating range further to see how much improvement is possible with a dynamic range of 0.1μA to 10.0μA, which should still give us the ability to resolve current differences to even greater accuracy. Fitting results give us a = 448614 and b = 0.859 with a correlation coefficient of 0.99999. Even though this restricted input current range produces a much better fit to the model, there is little to be gained by applying this input current range limit when we are only required to resolve current changes of the order of 1%. In all cases the self-stressing test structure cells use an unstressed structure reference point for comparison purposes.

The most demanding applications are the hot carrier degradation cells and the electromigration, version 2 cells. As can be seen from the model, it should be possible to easily resolve even 1% changes in measured parameter with proper timing in the controller that gates the current controlled oscillator output to the 16-bit counter used for measuring frequency.

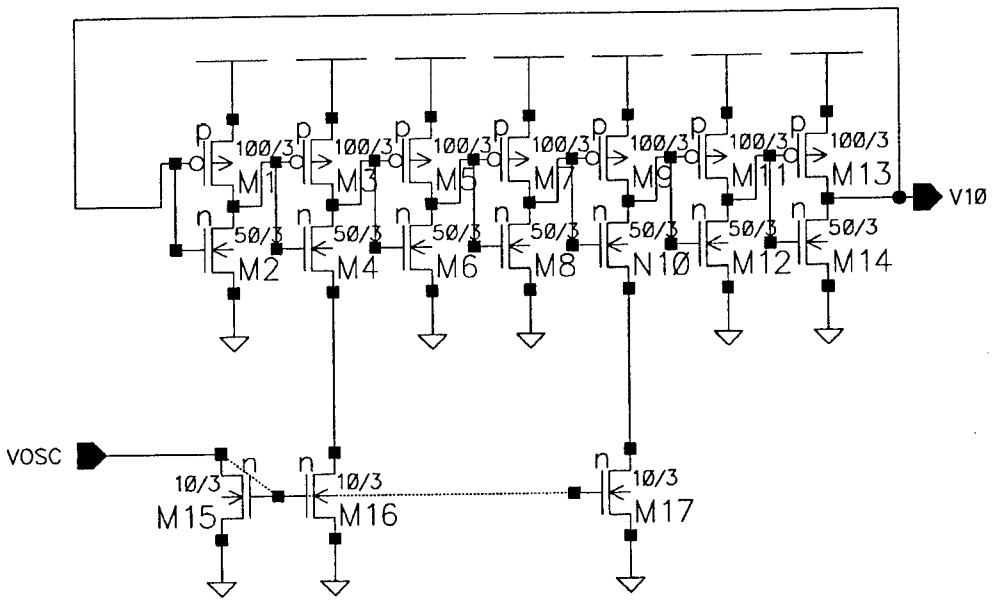


Figure A1: Current Controlled Oscillator - A simple current controlled oscillator is implemented using a ring oscillator with current controlled slew rate.

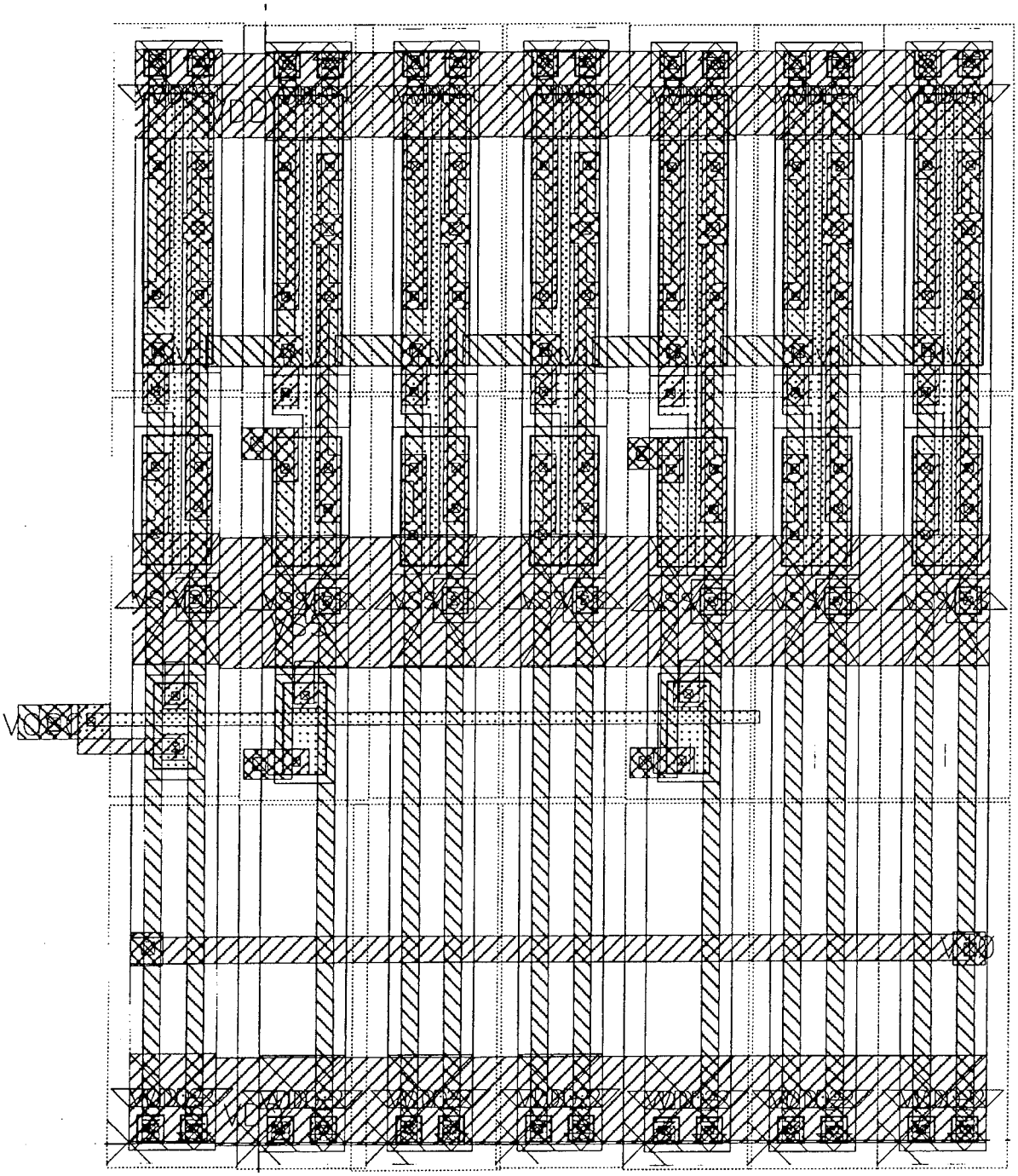


Figure A2: Current Controlled Oscillator Layout - This layout was constructed to conform to CMOSN standard cell form factors.

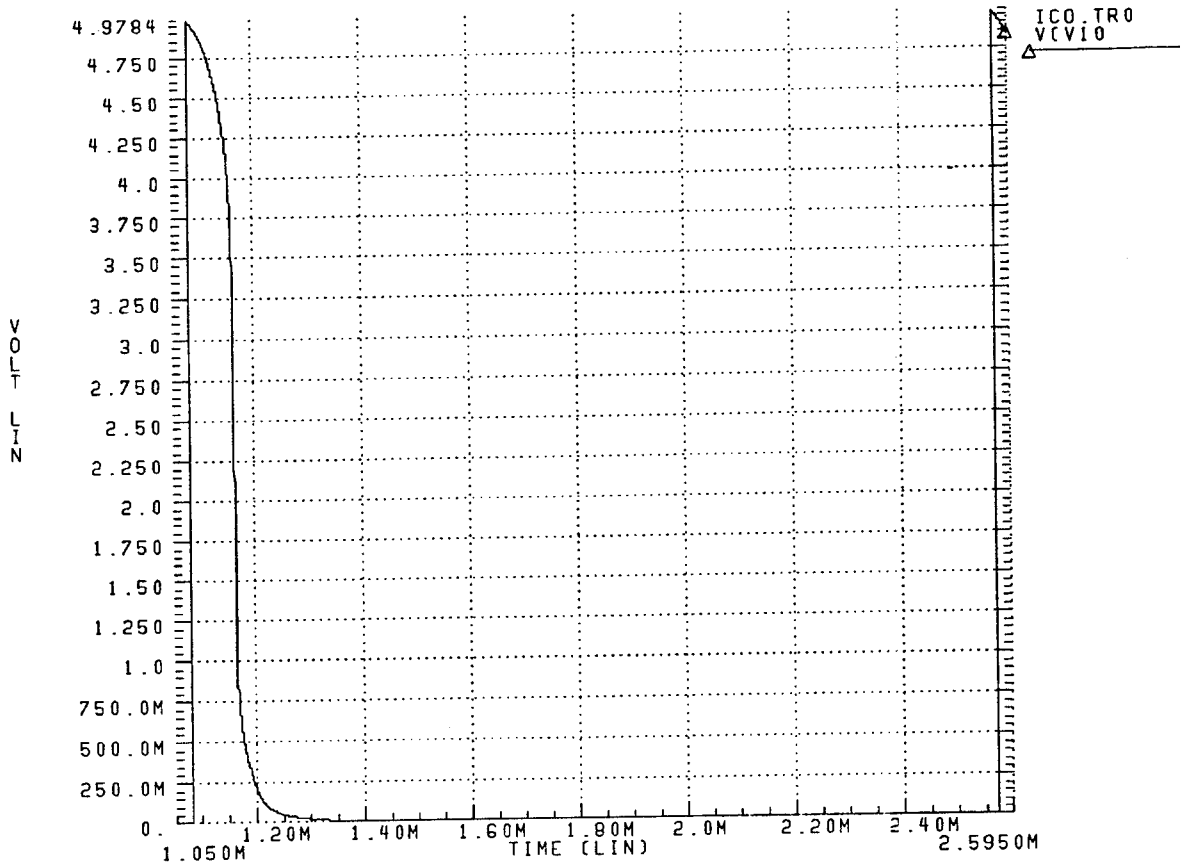


Figure A3a: CCO output waveform (single cycle) at input current of 0.001μA.

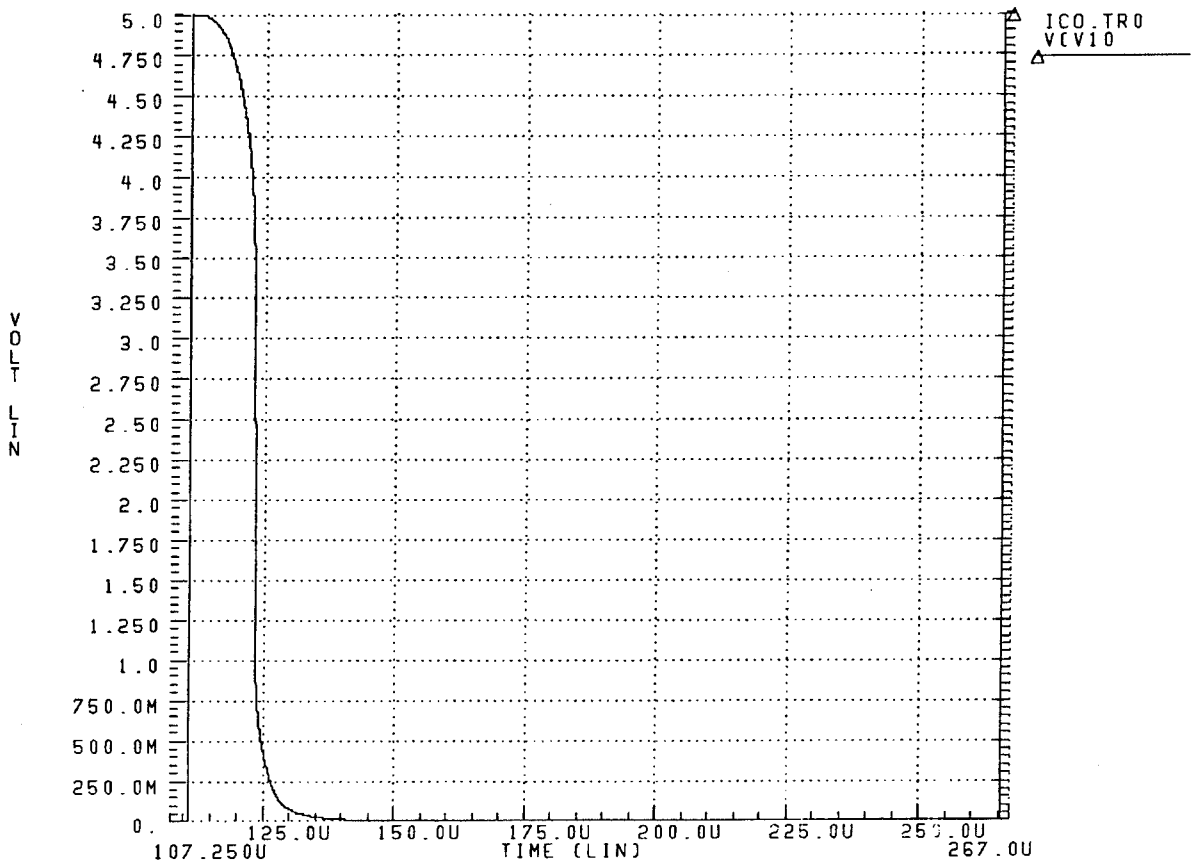


Figure A3b: CCO output waveform (single cycle) at input current of 0.01μA.

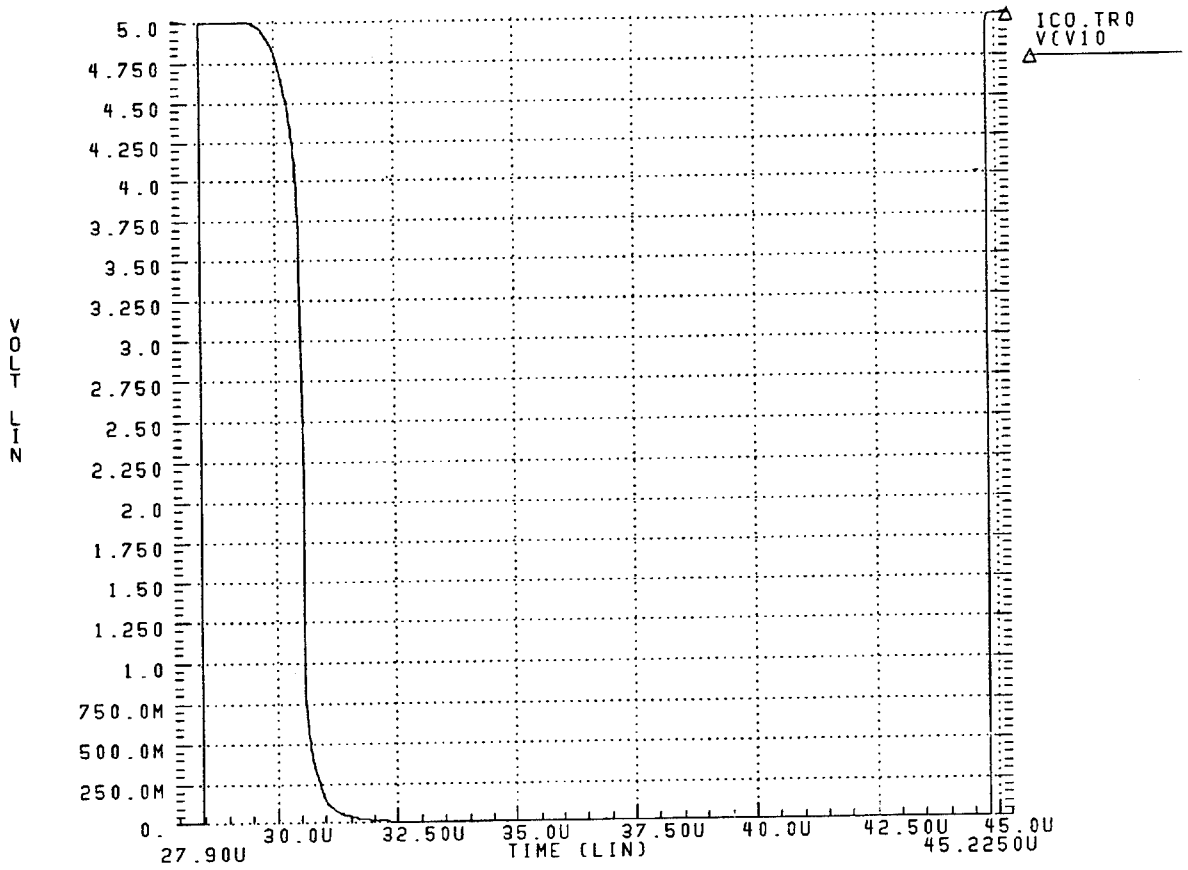


Figure A3c: CCO output waveform (single cycle) at input current of 0.1μA.

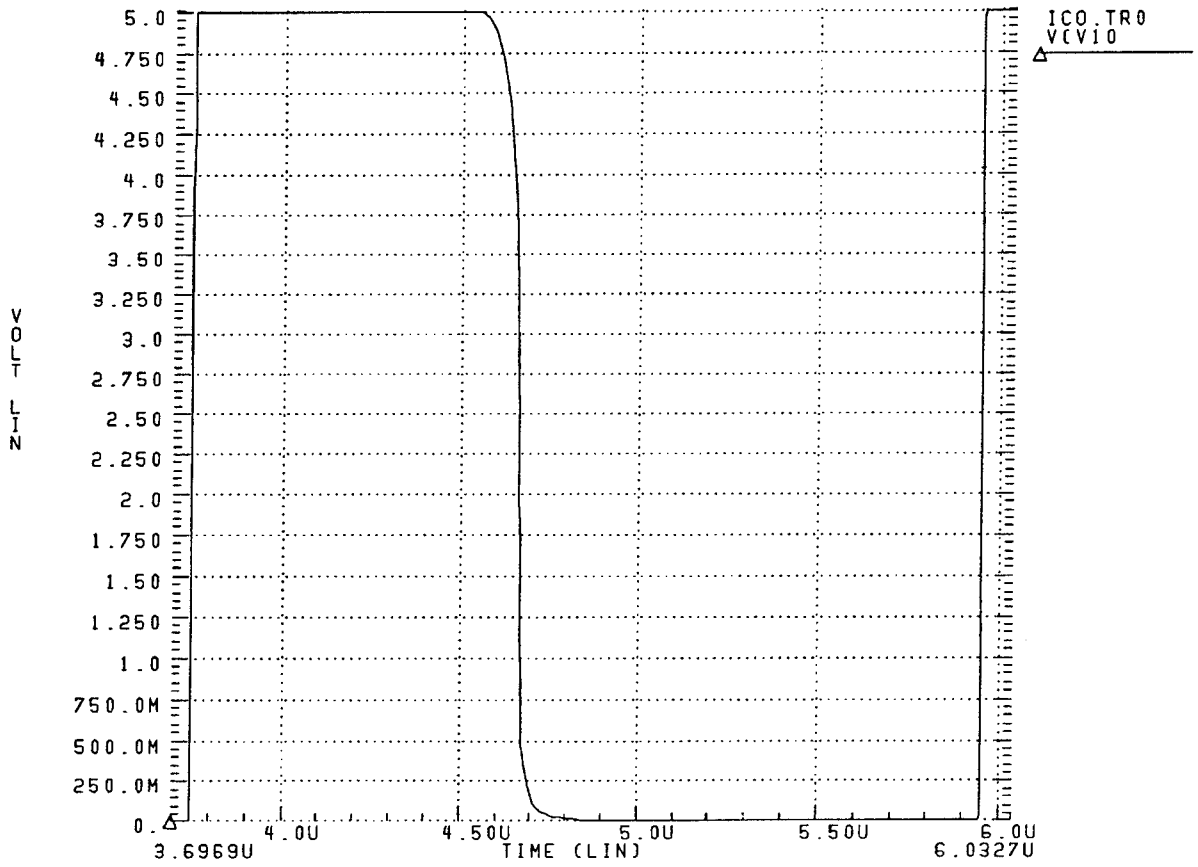


Figure A3d: CCO output waveform (single cycle) at input current of 1.0μA.

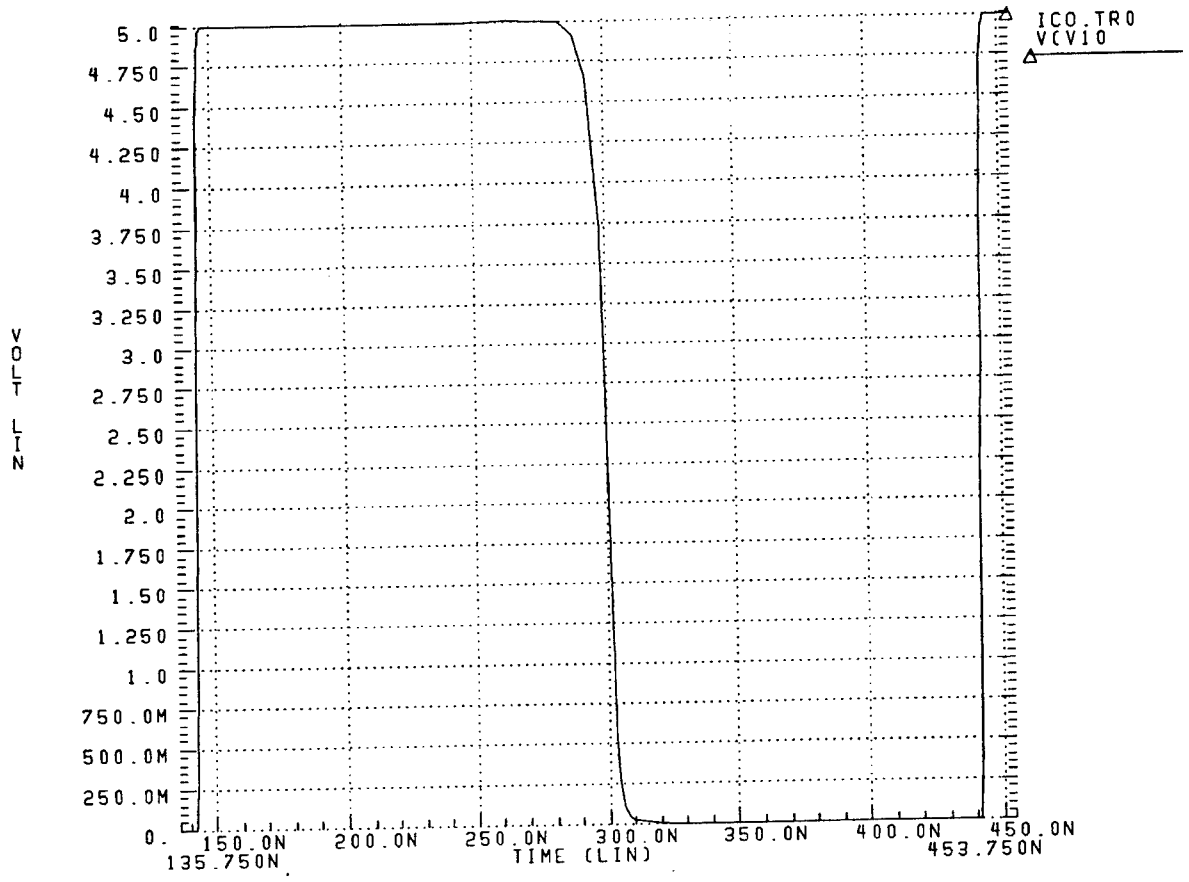


Figure A3e: CCO output waveform (single cycle) at input current of 10.0μA.

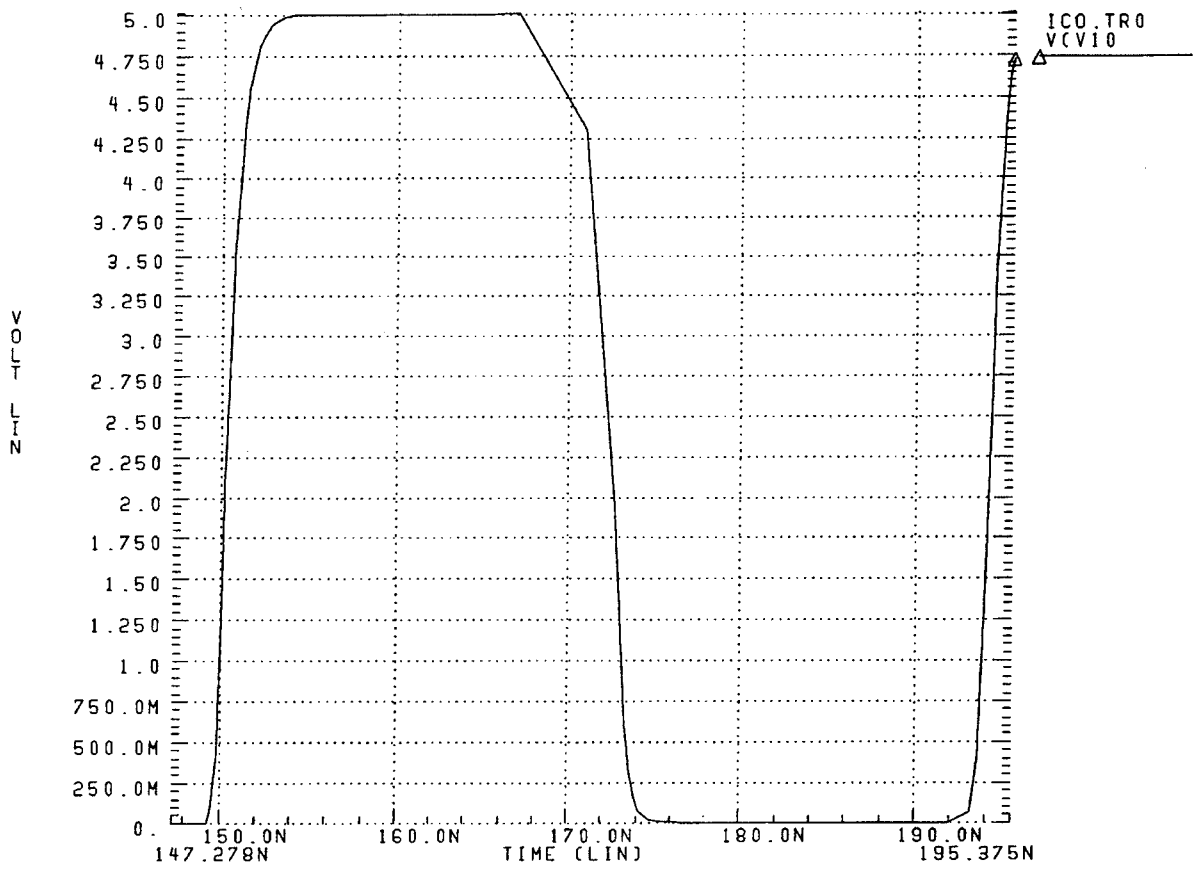


Figure A3f: CCO output waveform (single cycle) at input current of 100.0μA

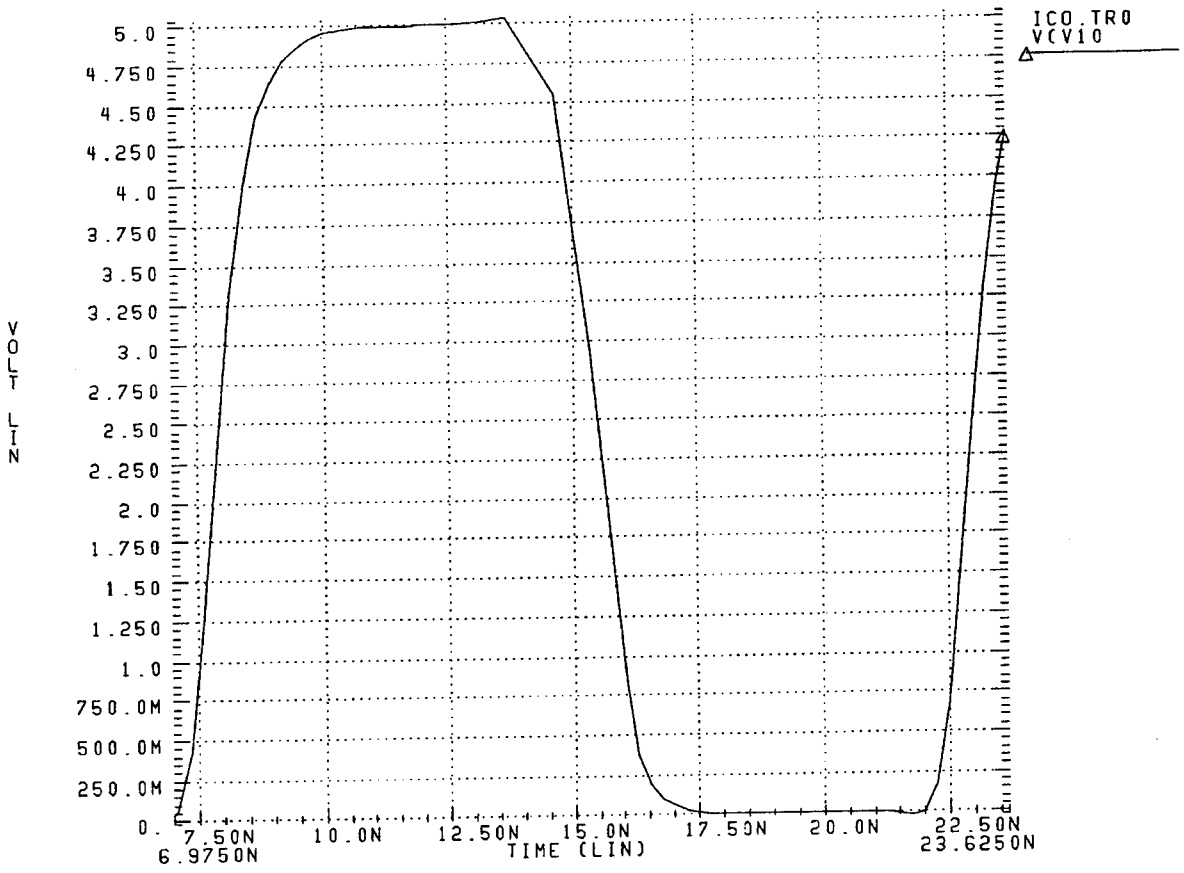


Figure A3g: CCO output waveform (single cycle) at input current of 1000μA

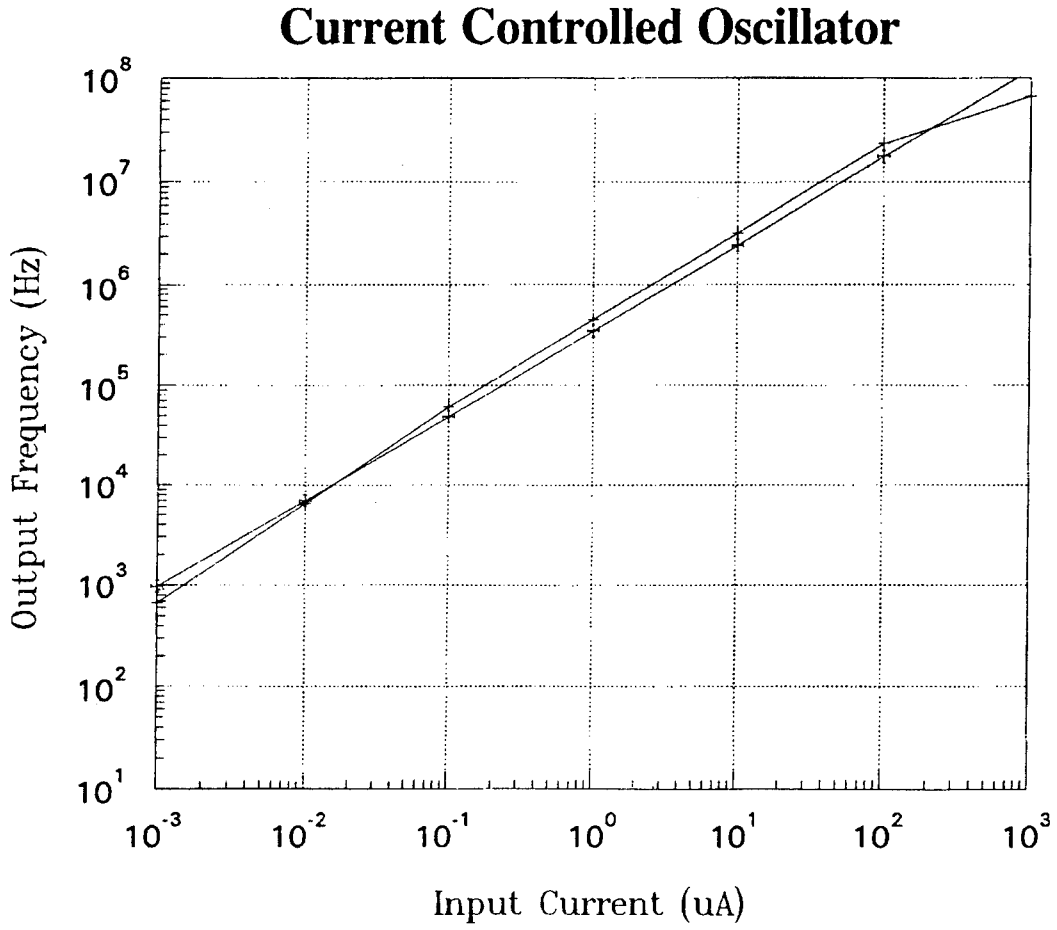


Figure A4a: CCO Frequency vs. Input current and fitting power function ($F = a*I^b$) over a current range of 0.001μA to 1000.0μA, where a = 347080, and b = 0.851 with a correlation coefficient of 0.996.

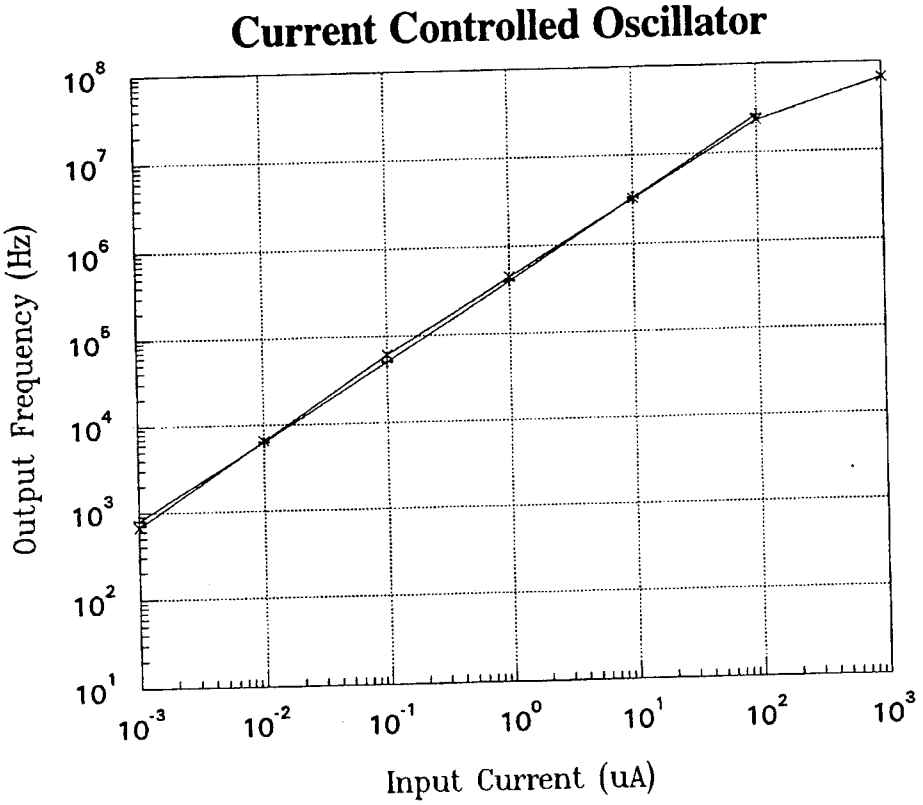


Figure A4b: CCO Frequency vs. Input current and fitting power function ($F = a*I^b$) over a current range of 0.001μA to 100.0μA, where a = 409694, and b = 0.905 with a correlation coefficient of 0.9994.

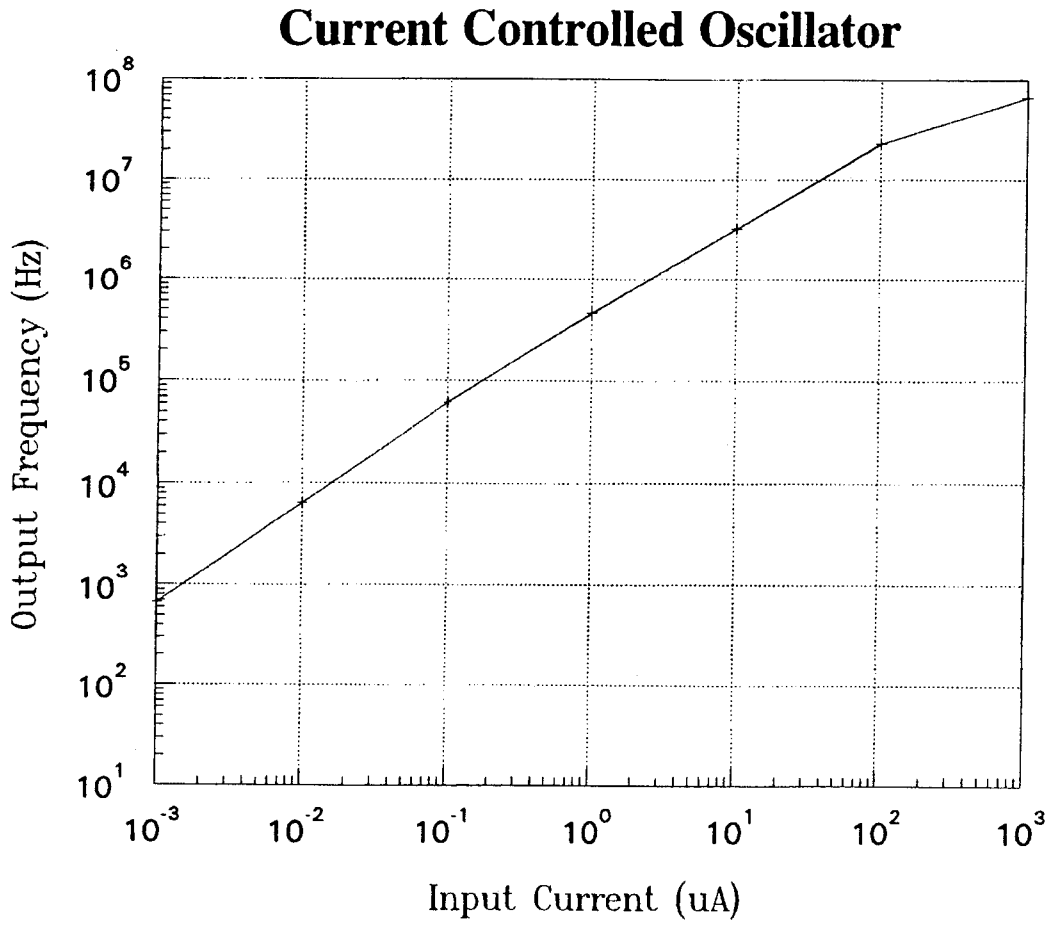


Figure A4c: CCO Frequency vs. Input current and fitting power function ($F = a*I^b$) over a current range of 0.1μA to 10.0μA, where a = 448614, and b = 0.859 with a correlation coefficient of 0.99999. Note that the fit function plot totally overlay the data in this region of the plot.

Appendix B

Time Dependent Dielectric Breakdown Cell

Time Dependent Dielectric Breakdown Cell

This appendix contains details of the TDDB self-stressing cell. The schematic diagram of the cell is in Figure B1, with the layout in Figures B2a and B2b. The plots that follow are from the SPICE simulations showing important characteristics of the cell performance. Two performance considerations are of note here: 1) The amount of time delay that is required for detection of a "leaky" gate oxide capacitor that exhibits a large shunt resistance. 2) The final boost voltage from the well bias generator which supplies the above normal stress voltage that tests the gate oxide quality.

The first plot (figure B3) shows that the rise time to 6.0 Volts is about 10μs. The time interval at the end of the transient simulation shows that the ultimate voltage boost is about 6.5 Volts after about 200μs. This is a typical value of voltage boost that can be generated by this circuit when used in a nominal CMOS fabrication process that is optimized for digital applications.

By changing the SPICE simulation to include a 500KΩ shunt resistance to ground at the voltage boosted well we can explore the settling time required to detect an oxide breakdown that results in a high shunt resistance. Simulation results (Figure B4) indicate that the voltage decay time to a detectable threshold is in the range of 50μs to 80μs. If we are going to allow for this special oxide breakdown case there must be a measurement delay after the bias generator is disabled.

The last simulation plot (Figure B5) shows that there is not a low resistance leakage path in the design that would cause a false oxide failure indication. The test conditions are that the well bias generator is operated for a short period of time and then disabled while watching for a decline in well voltage caused by any circuit leakage paths. In any real circuit there will be leakage current through the reverse biased junctions, current flow through "off" transistors because of subthreshold conduction and, to some extent, Fowler-Nordheim current flow through the in-tact gate oxide. We did not attempt to simulate the primary leakage paths because SPICE models junction leakage and subthreshold conduction poorly. It is probably prudent to limit measurement delay to less than 1.0ms to guard against false oxide failure indication by junction leakage at high temperature.

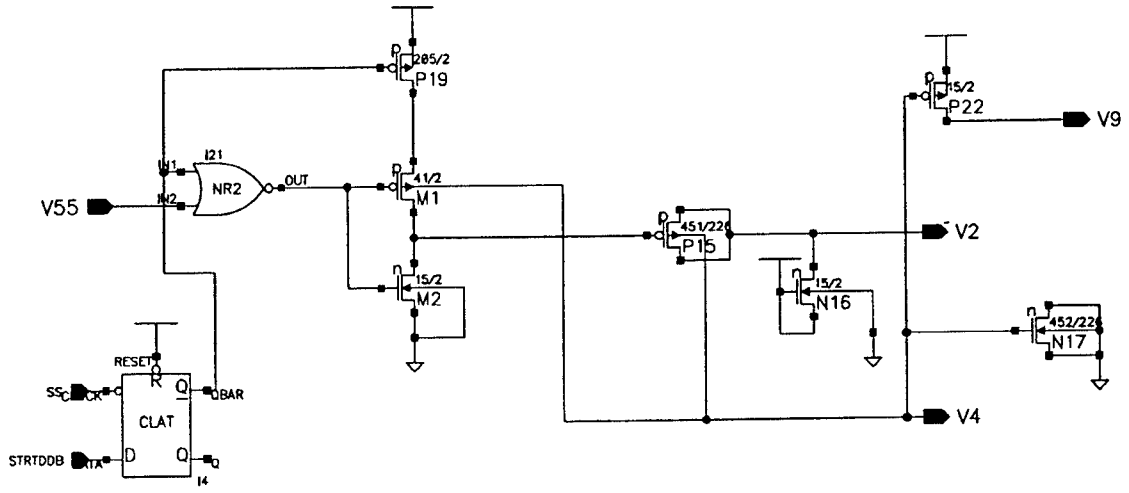


Figure B1: TDDB Self-Stressing Cell Schematic Diagram - This circuit extraction from layout does not show the parasitic diode that transistor P15 provides to the N-well. Transistor N16 functions as a diode to the Vdd rail.

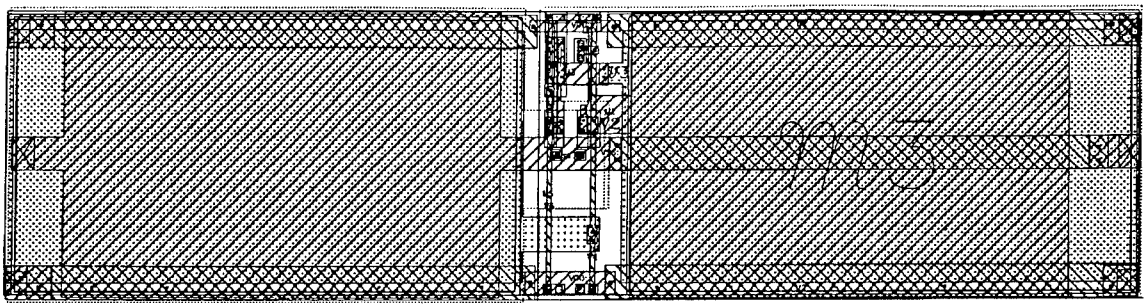


Figure B2a: TDDB Self-Stressing Cell Well Bias Generator Layout - This is the basic well bias cell. It must be combined with the standard cell NOR gate and state flip-flop to produce the final test structure.

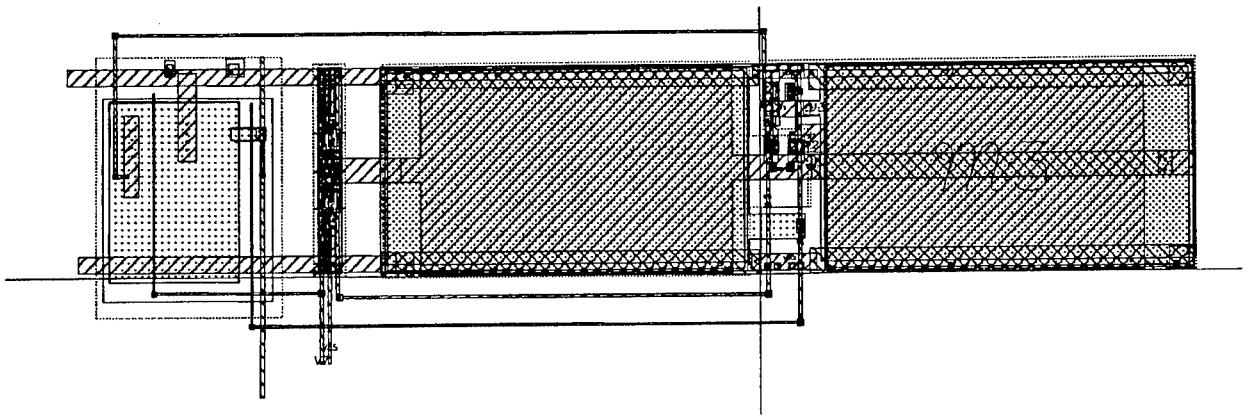
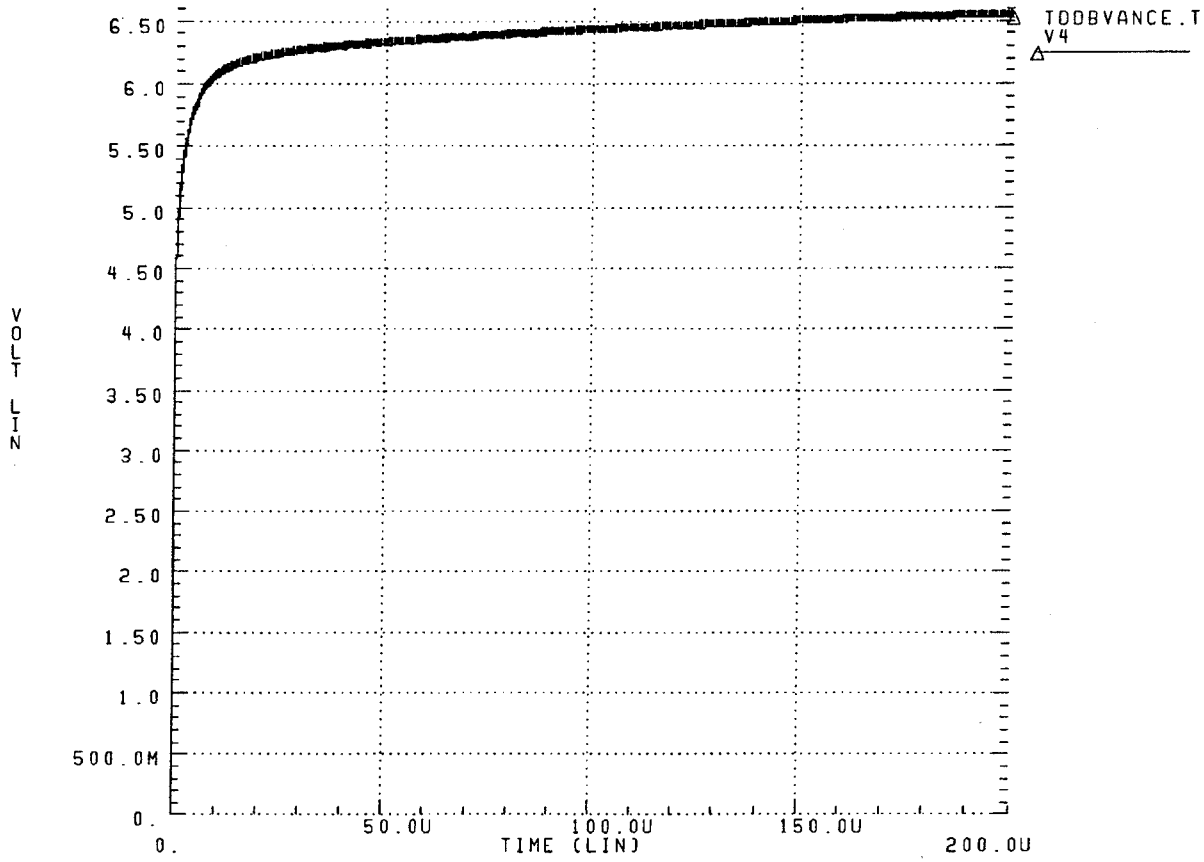


Figure B2b: TDDB Self-Stressing Cell Layout - Note that the test structure area is dominated by the large test capacitors in the well bias generator.



B3: Figure Simulator output of the TDDB Self-Stressing Sell well bias generator.

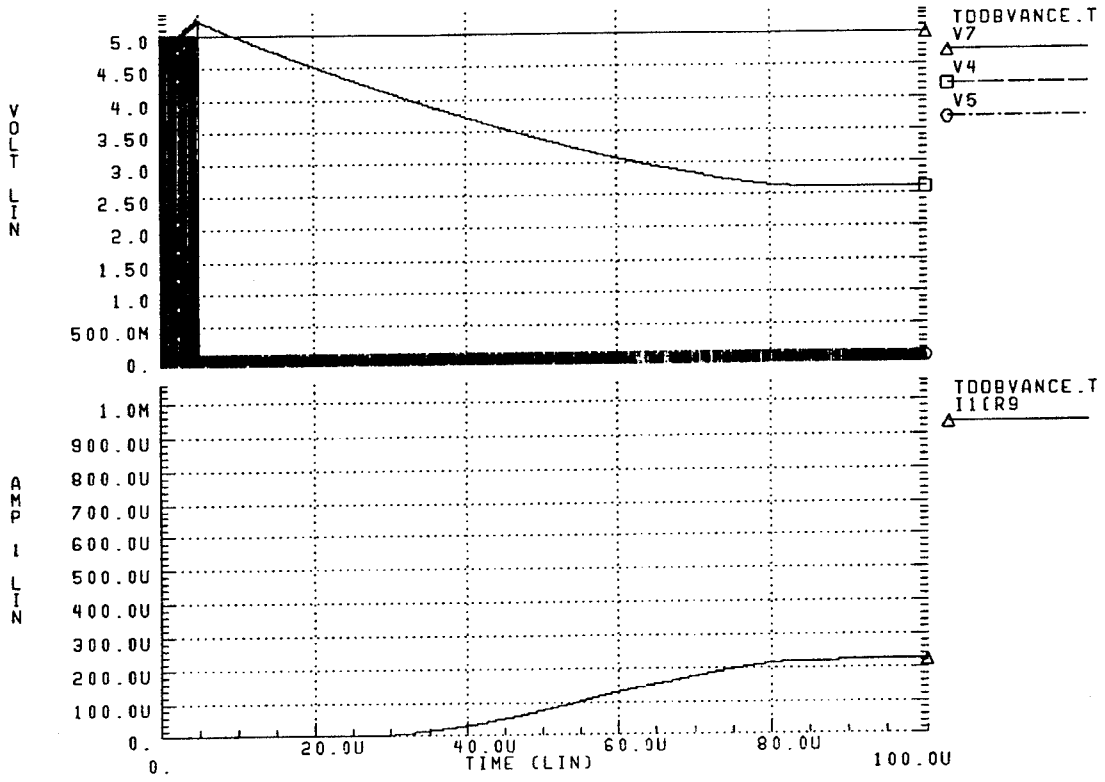


Figure B4: High capacitor leakage resistance failure - This simulation shows the time delay between switching to test mode to the indication of failure detect transistor output current. The circuit reaches an unambiguous failure indication at about 80μsec. after entering test mode.

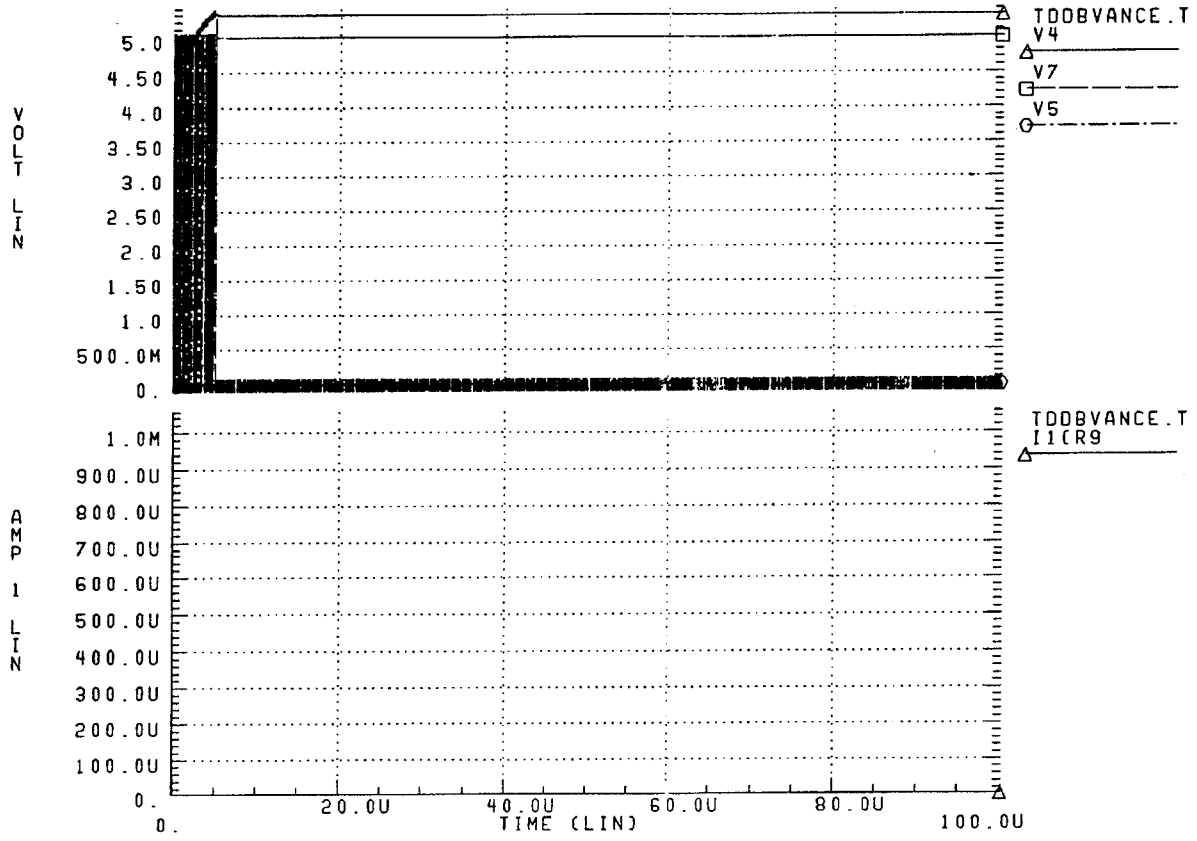


Figure B5: This simulation output shows no failure detect current when there is no test capacitor leakage path. Note that the SPICE model equations do not adequately model diode leakage and subthreshold leakage, so this simulation does not accurately provide an upper bound for measurement delay time after entering measurement mode.

Appendix C

Hot Carrier Damage Cell

Hot Carrier Damage Cell

This appendix contains details of the hot carrier damage self-stressing test structure cell. The schematic diagram of the cell is in Figure C1. We are primarily concerned with the ability to resolve relative differences in saturation current between two transistors, one that has been subjected to hot carrier stress bias conditions, and the other that is only used for reference. SPICE simulation comparisons were possible because we were able to generate a number of sets of SPICE model parameters for N-channel transistors that have been subjected to various amounts of accelerated hot carrier stress bias. The SPICE model parameters for transistors subjected to stress conditions of Vdd = 7.0 Volts, Vgs = 2.1 Volts for 100sec., 1000sec., and 10000sec. are contained in Figure C2. A g_m degradation plot is included in Figure C3, which shows the typical degradation in transistor performance at the above stress conditions.

Looking at the schematic diagram, it should be noted that critical transistors involved in the process of saturation current comparison are shown as two transistors in parallel. Parallel pairs are: test transistor current mirror (P44 parallel with P66; P67 parallel with P45), reference transistor current mirror (P68 parallel with P46; P69 parallel with P47), the test transistor (N63 parallel with N48) and the reference transistor (N51 parallel with N64). This is a reminder that the layout is constructed to have some spatial diversity in the layout of these transistors to reduce the mismatch between the test transistor and its reference transistor and between the two current mirrors that are used to measure the saturation current of both transistors. The current mirrors are ratioed to allow reduction of the saturation current without saturating the current controlled oscillator. The two pairs of P-channel devices in the two current mirrors are constructed in a simple common centroid layout. Layouts of the test transistor and the reference transistor are done in a similar manner. Layout of the basic hot carrier cell is included in Figure C4. A common centroid layout was considered unnecessary for the mode switch transistors.

Figures C5, C6, C7, and C8 contain the simulation plots of the current mirror output current for a test transistor that has been unstressed and stressed at the above conditions for 100sec., 1000sec., and 10000sec. respectively. It clearly illustrates that if the test transistor suffers hot carrier stress damage, even at the test voltages used for the self-stressing hot carrier structure, the resulting change in drain current is measurable as a change in current relative to the reference transistor.

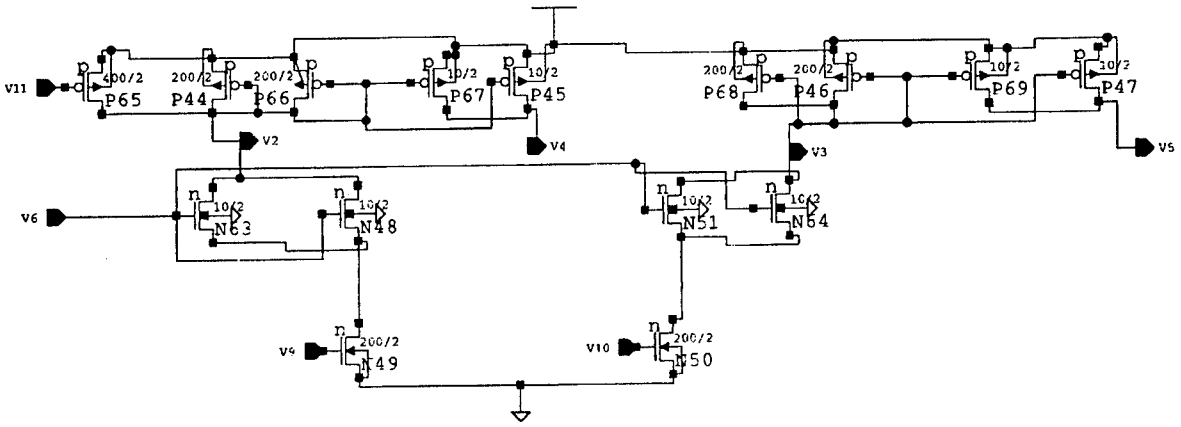


Figure C1: Self-stressing Hot Carrier Damage Cell Schematic Diagram - The circuit extracted schematic shows parallel connected transistors indicating the presence of the common centroid layout.

* Transistor Parameters Before Hot Carrier Stress.	* Transistor Model Parameters after 100 Seconds of Stress.
.MODEL N0 NMOS LEVEL=2 LD=0.250000U +TOX=403.000001E-10 NSUB=2.624877E+16 VTO=0.985672 +KP=5.698400E-05 GAMMA=1.0894 PHI=0.6 UO=665 +UEXP=0.241232 UCRIT=99944 DELTA=1.93174 VMAX=79985.2 +XJ=0.250000U LAMBDA=2.618041E-02 NFS=3.910000E+11 +NEFF=1 NSS=1.000000E 10 TPG=1.000000 RSH=23.080000 +CGDO=3.213223E-10 CGSO=3.213223E-10 CGBO=3.502129E-10 + CJ=3.777700E-04 MJ=0.445282 CJSW=5.017100E-10 +MJSW=0.365853 PB=0.800000 * Weff = Wdrawn - Delta_W * The suggested Delta_W is 0.02 um	.MODEL N100 NMOS LEVEL=2 LD=0.250000U +TOX=403.000001E-10 NSUB=2.383091E+16 VTO=0.991256 +KP=5.394000E-05 GAMMA=1.038 PHI=0.6 UO=629.96 +UEXP=0.227687 UCRIT=97729.7 DELTA=2.33156 +VMAX=71558.4 XJ=0.250000U LAMBDA=3.497039E-02 + NFS=3.910000E+11 NEFF=1 NSS=1.000000E+10 TPG=1.000000 + RSH=23.080000 CGDO=3.213223E-10 CGSO=3.213223E-10 +CGBO=3.502129E-10 CJ=3.777700E-04 MJ=0.445282 +CJSW=5.017100E-10 MJSW=0.365853 PB=0.800000 ** Weff = Wdrawn - Delta_W ** The suggested Delta_W is 0.02 um
* Transistor Model Parameters after 1000 seconds of stress.	* Transistor Model Parameters after 10000 seconds of stress.
.MODEL N1000 NMOS LEVEL=2 LD=0.250000U +TOX=403.000001E-10 NSUB=2.066375E+16 VTO=1.11296 +KP=5.390000E-05 GAMMA=0.9666 PHI=0.6 UO=629 +UEXP=0.245897 UCRIT=93279.7 DELTA=8.10723 +VMAX=63399.4 XJ=0.250000U LAMBDA=5.603452E-02 + NFS=3.910000E+11 NEFF=1 NSS=1.000000E+10 TPG=1.000000 + RSH=23.080000 CGDO=3.213223E-10 CGSO=3.213223E-10 +CGBO=3.502129E-10 CJ=3.777700E-04 MJ=0.445282 +CJSW=5.017100E-10 MJSW=0.365853 PB=0.800000 * Weff = Wdrawn - Delta_W * The suggested Delta_W is 0.02 um	.MODEL N10000 NMOS LEVEL=2 LD=0.250000U +TOX=403.000001E-10 NSUB=2.066375E+16 VTO=1.06148 +KP=4.798000E-05 GAMMA=0.9666 PHI=0.6 UO=560.299 +UEXP=0.204945 UCRIT=104374 DELTA=10.3537 +VMAX=48773.2 XJ=0.250000U LAMBDA=6.745434E-02 + NFS=3.910000E+11 NEFF=1 NSS=1.000000E+10 TPG=1.000000 + RSH=23.080000 CGDO=3.213223E-10 CGSO=3.213223E-10 +CGBO=3.502129E-10 CJ=3.777700E-04 MJ=0.445282 +CJSW=5.017100E-10 MJSW=0.365853 PB=0.800000 * Weff = Wdrawn - Delta_W * The suggested Delta_W is 0.02 um

Figure C2: Transistor SPICE model parameters for N-channel transistors that have various amounts of hot carrier damage. Stress bias conditions are Vdd = 7.0V., Vgs = 2.1V. for stress times of 0.0sec., 100sec., 1000sec., and 10,000sec.

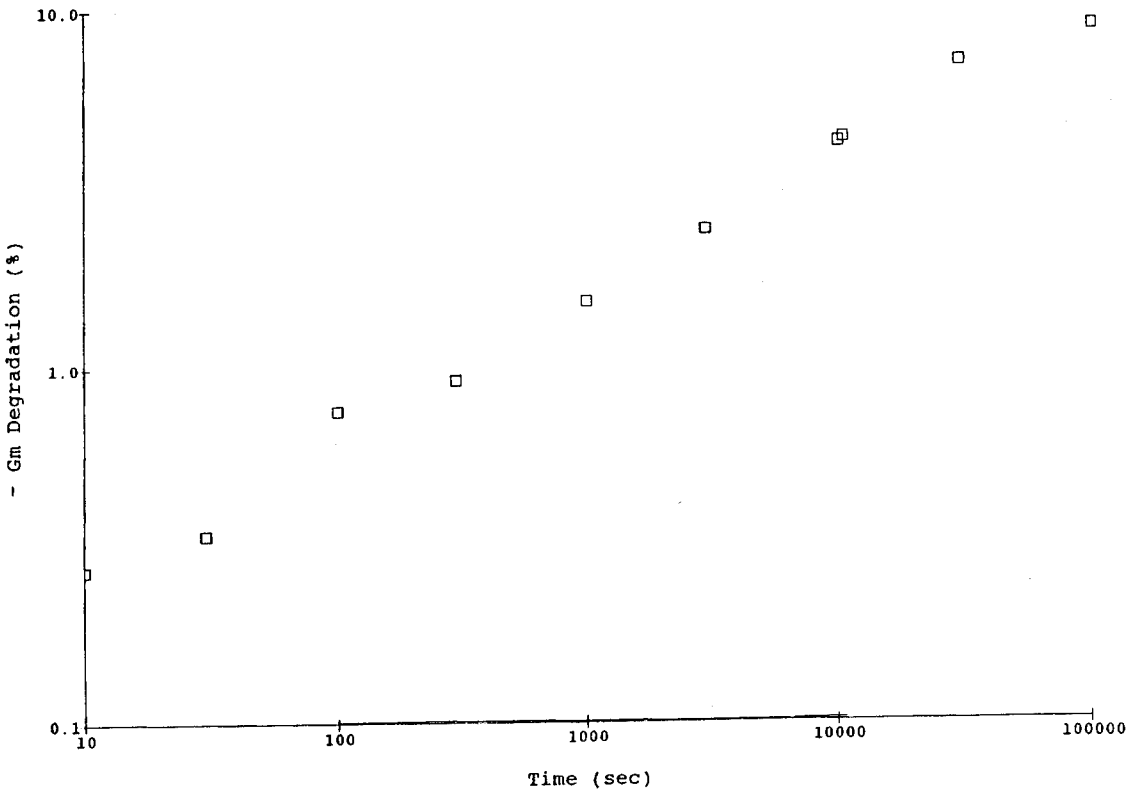


Figure C3: Plot of measured g_m degradation after hot carrier stressing at indicated bias conditions for various stress time periods.

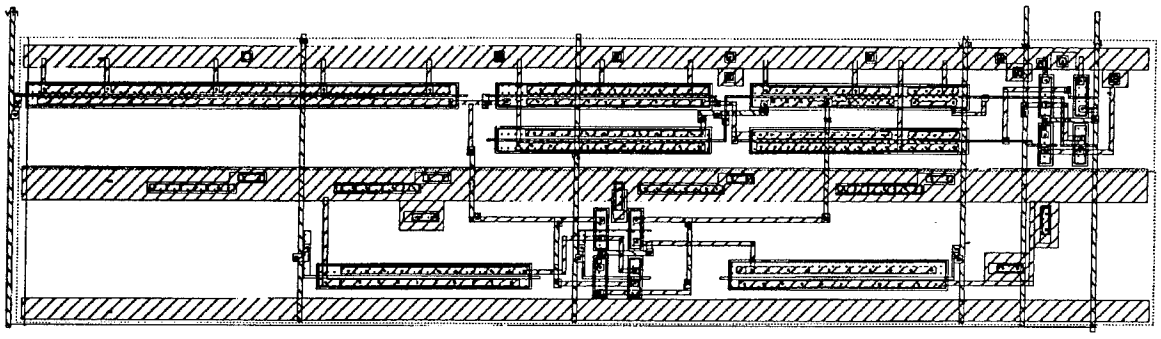


Figure C4: Hot Carrier Damage Self-Stressing Cell Layout - A simple common centroid layout is used to reduce the small transistor parametric variations that occur in different chip locations. Since this test structure was designed for use in a digital CMOS process, these parametric variations can be significant when looking for small saturation current differences.

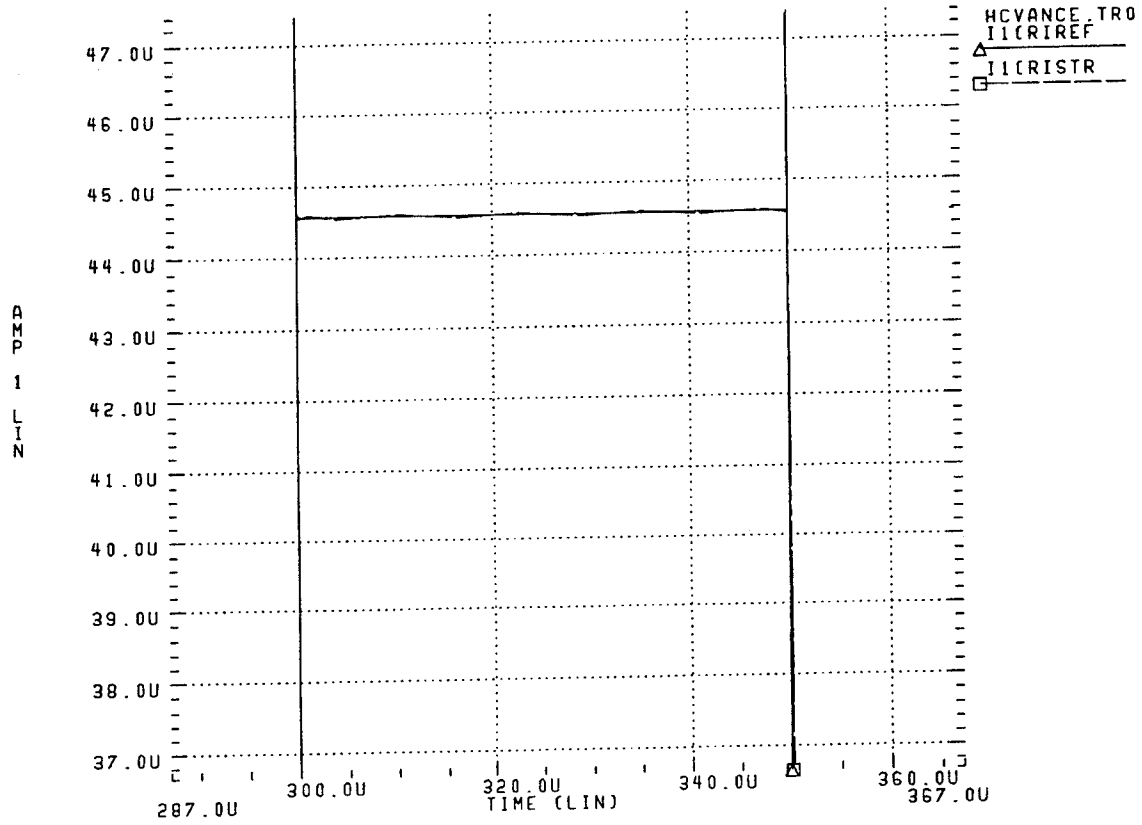


Figure C5: Hot Carrier Damage Cell Simulation - Before hot carrier stress.

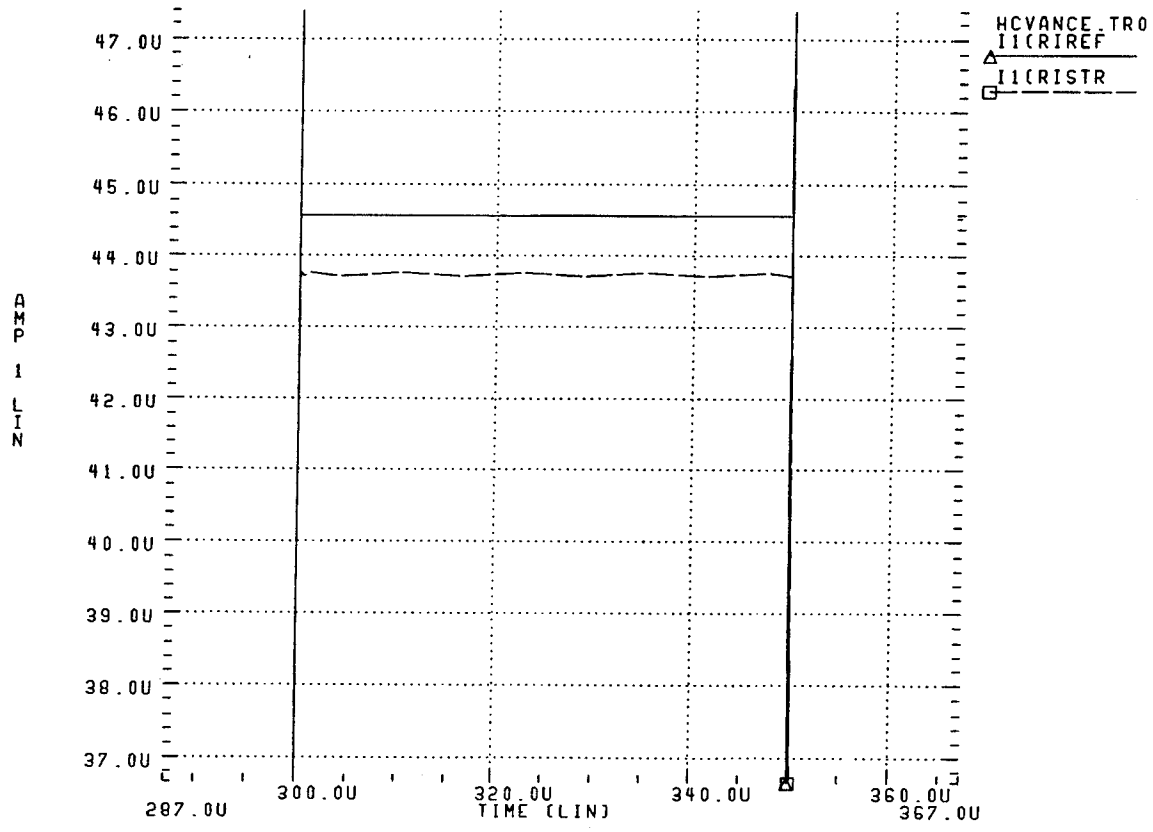


Figure C6: Hot carrier Damage Cell Simulation - After hot carrier stress at Vdd = 7.0 V., Vgs = 2.1 V. for 100 seconds. Note slightly less than 2% drop in saturation current in the stressed transistor compared with the unstressed device.

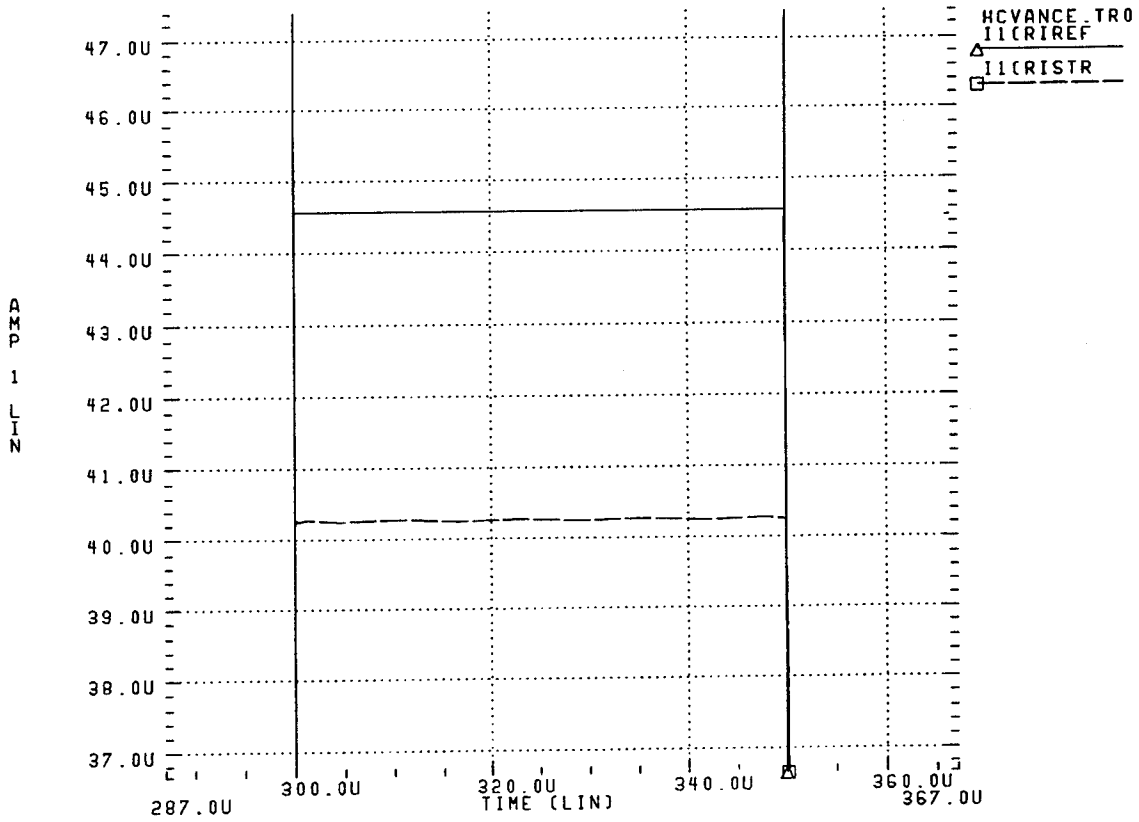


Figure C7: Hot carrier Damage Cell Simulation - After hot carrier stress at Vdd = 7.0 V., Vgs = 2.1 V. for 1000 seconds. Note slightly less than 10% drop in saturation current in the stressed transistor compared with the unstressed device.

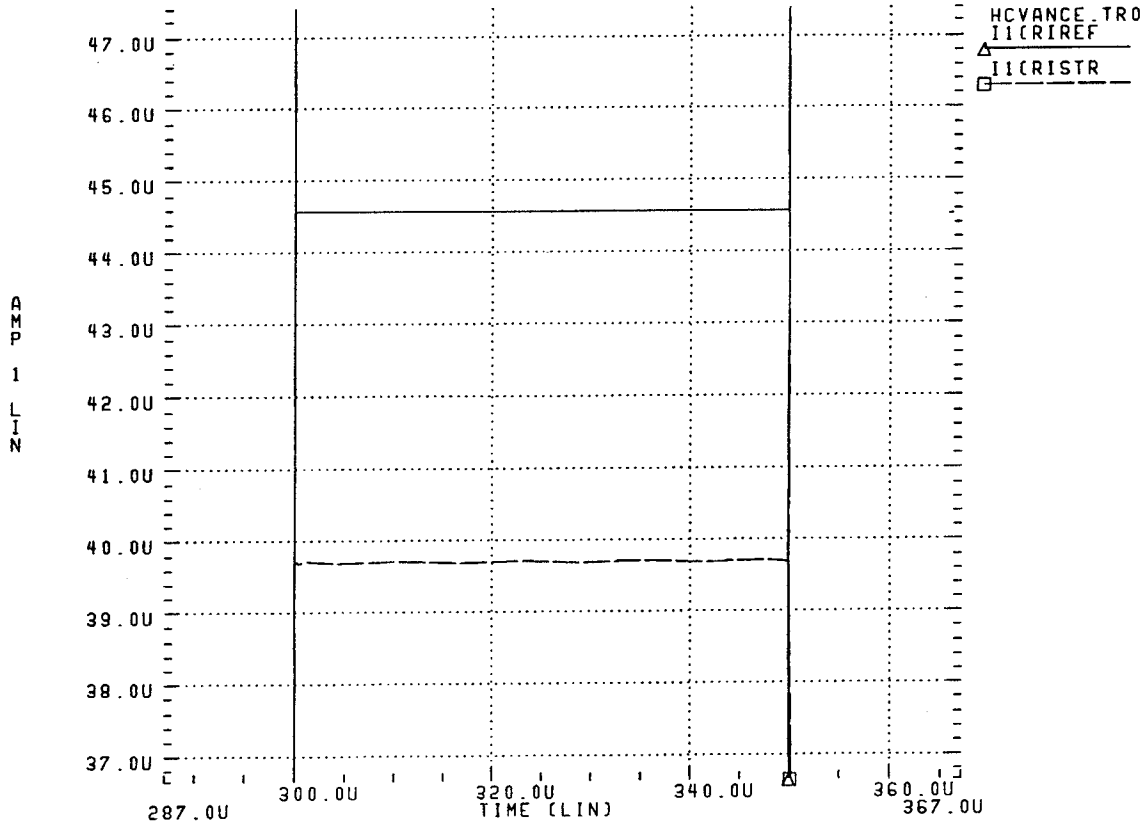


Figure C8: Hot carrier Damage Cell Simulation - After hot carrier stress at Vdd = 7.0 V., Vgs = 2.1 V. for 10,000 seconds. Note slightly more than 10% drop in saturation current in the stressed transistor compared with the unstressed device.

Appendix D

Electromigration Cell

Version 1, 2

Electromigration Cell

This appendix contains details of the Electromigration self-stressing cell. The electromigration test structure has been implemented in two versions: Version 1, which is optimized for minimum area and with metal open circuit detect only; and Version 2 which is designed to be able to detect small relative resistance changes. Both versions were created so that an area/performance tradeoff is possible when working with simple uniform aluminum alloy metal systems and complex composite metal systems. In both versions the stress factor is only moderate in order to conserve power to the cell.

Version 1:

The schematic and layout of the Version 1 electromigration test cell is divided into three portions: 1) Resistor Array, Figures D1 and D2. 2) Failure Detector Multiplexer, Figures D3 and D4. 3) Test Control Logic, Figures D5 and D6. Verification of these circuits involve only a little more than switch level simulation.

Simulation results from this design are essentially single point solutions because the only failure mode that is detectable is an open resistor segment. If a segment is open, then the fail detect current source is enabled which results in a fixed current output. This fixed current is sensed by the current controlled oscillator as a high frequency output. Simulations of the functionality of the Failure Detector Multiplexer show correct multiplex operation as well as expected failure detect current output.

Verification of the Test Control Logic can be either done with logic simulations or SPICE simulations. The design and layout of this function was accomplished with CMOSN standard cells with a commercial CAD system. It was only necessary to verify that the correct address decode occurred.

Version 2:

The schematic and layout of Version 2 electromigration test cell is in two parts: 1) Resistor array - measurement multiplexer. 2) Test Control Logic. The major difference between Version 1 and Version 2 is that Version 2 must include the capability of selecting each resistor segment for resistance measurement with the Current Controlled Oscillator, which requires that the current source to be measured be reflected out of the Vdd rail. It was therefore necessary to combine the resistor array with the measurement multiplexer. Figure D7 contains the schematic of the Resistor Array - Measurement Multiplexer. The schematic Test Control Logic is on Figure D8 and its layout is in Figure D9. The only change required relative to Version 1 Test Control Logic is the addition of a flip-flop and two NAND gates to select the high and low points of the resistor under test and to disable any output from the Resistor array - measurement multiplexer.

The circuit design of this electromigration test cell involves the use of some rather large channel width P-channel transistors that are used to pull the high end of each resistor segment to near Vdd potential. The 2000μm channel width was dictated by the fact that the transistor dynamic impedance must be substantially smaller than the 31Ω resistance of a resistor segment. Since seven of these large transistors are required for this design, the transistors will have significantly larger area than the resistor array itself. SPICE simulation results of different state configurations of the Measurement Multiplexer are found in Figures D10a - D10b and D11a - D11b. The different state configurations

tested are: 1) TR1_ low to enable testing of R1 before and after electromigration stress. 2) TR7_ low to enable testing of R7 before before and after electromigration stress. 3) No resistor selected to test the compliance of the current mirror that supplies test current and measurement current (which shows the drain of the current regulatior transistor at about 2.7 Volts). Figures D10a and D10b show resistors before electromigration stress. Another simulation included in Figures D11a - D11b which has R1 and R7 set to a resistance that is 10% higher than the first simulation (34.1Ω) to simulate electromigration caused resistance increase. By comparing the difference in output current (through the 100KΩ resistor) of the before electromigration simulation (R1: 46.1μA - 43.3μA = 2.8μA; R7: 40.8μA - 38.0μA = 2.8μA) with the after electromigration simulation (R1: 46.1μA - 43.0μA = 3.1μA; R7: 40.7μA - 37.6μA = 3.1μA) we can see that the resistance of R1 and R7 has indeed increased by about 10%. In the actual cell with the current being sampled by the Current Controlled Oscillator the current difference numbers above would actually be frequency differences. This shows that as long as each resistor before significant stressing is compared against the same resistor after stressing resistance changes of the order of 10% are easily detected despite the fact that the stress/measurement current source output changes depending upon how many resistors are bypassed by the transistor switches. This also underscores the importance of conducting the resistance change tests under the same environmental conditions (ambient temperature, chip Vdd, and chip power dissipation in particular) in order to avoid interference from these significant contributions. The measurement scheme implemented here is capable of remarkable sensitivity despite the lack of voltage and current references other than chip supply voltage.

The schematic of the Test Control Logic is in Figure D12 and is only a slight modification of the Version 1 Test Control Logic.

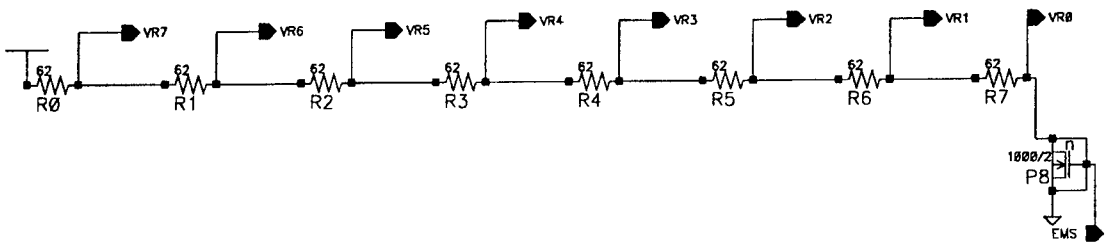


Figure D1: Version 1 Metal Resistor String Schematic - Includes the stress current switch transistor. Current is limited by the total resistor string resistance at Vdd = 5.0 Volts.

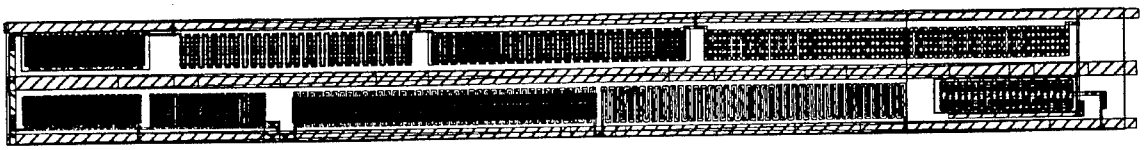


Figure D2: Version 1 Metal Resistor String Layout - A large area structure compared with other self-stressing cells.

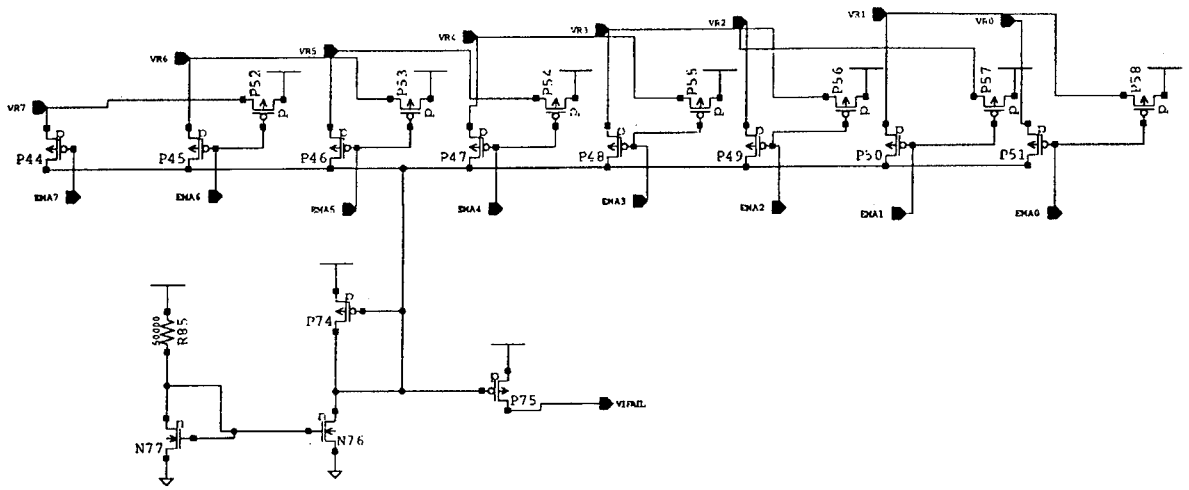


Figure D3: Version 1 Failure Detector Multiplexer - Only open circuit metal line failures are detectable with this circuit.

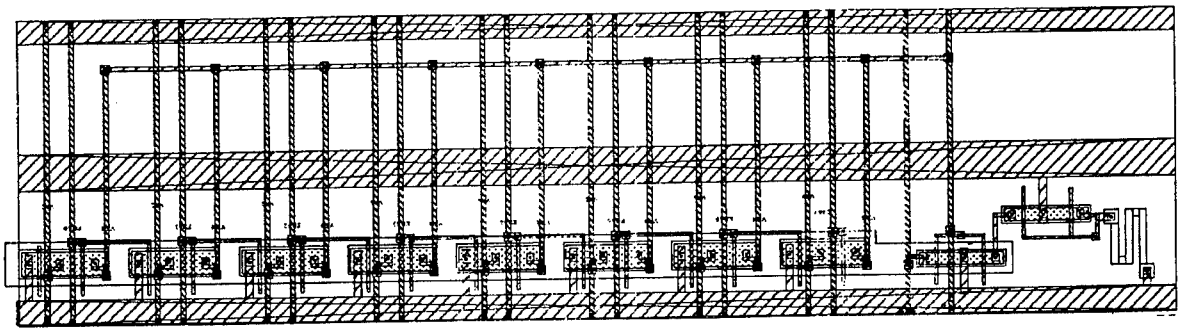


Figure D4: Layout of Failure Detector Multiplexer Cell, Version 1.

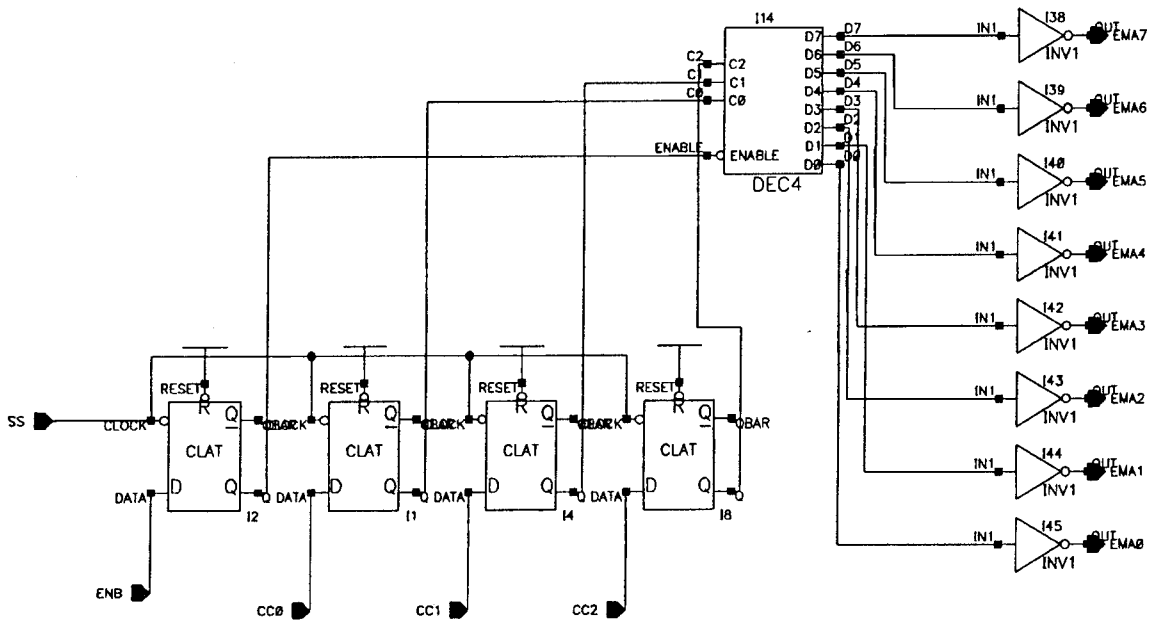


Figure D5: Version 1 Multiplexer Address Latch and Decoder Logic Diagram.

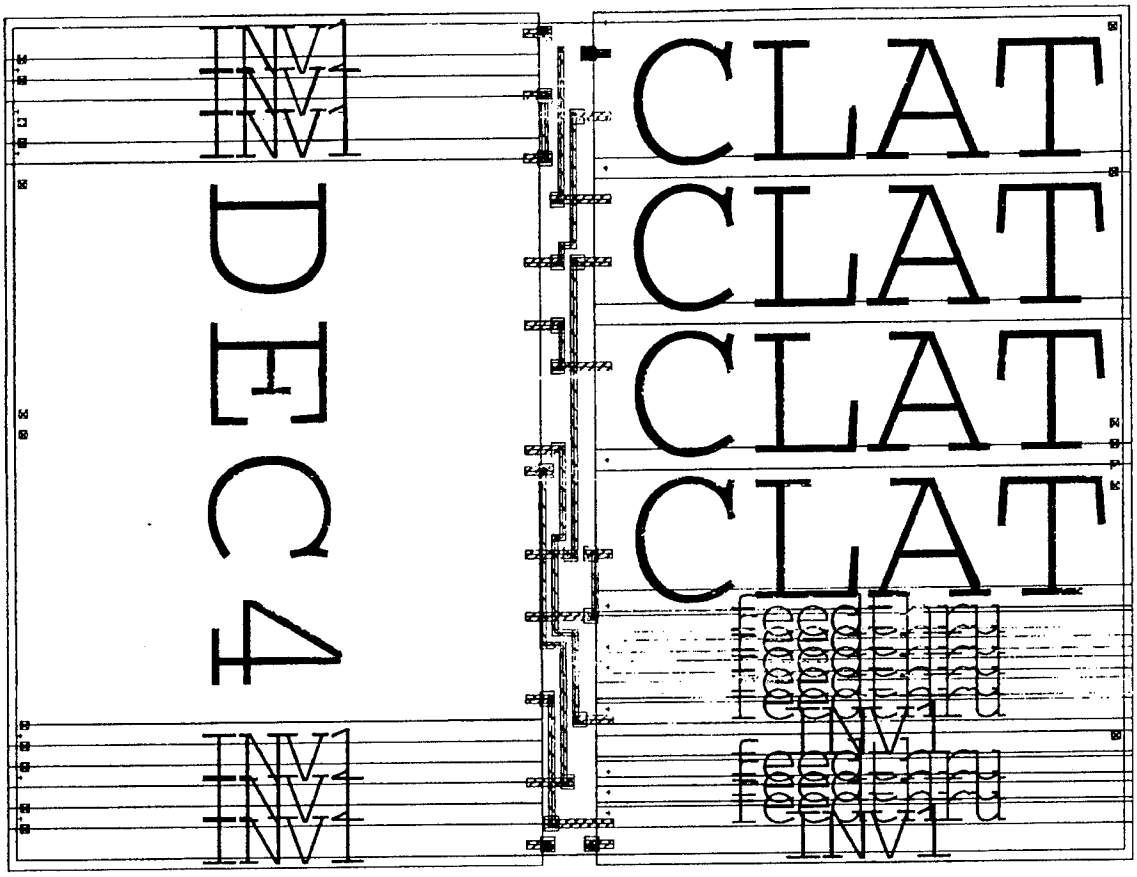


Figure D6: Test Control Logic Standard Cell Placement Block and Cell Interconnect. Layouts of the individual standard cells are omitted.

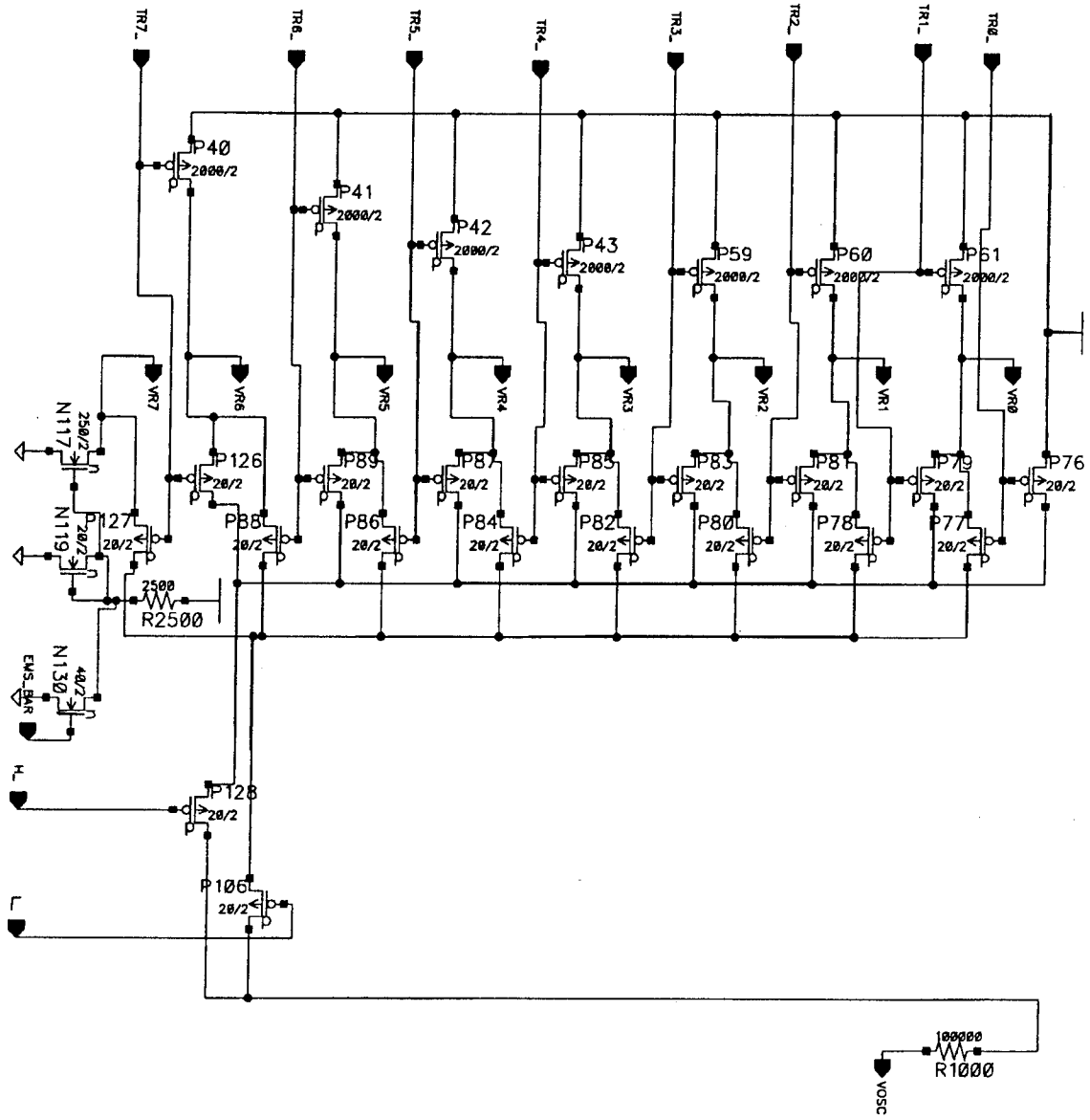


Figure D7: Version 2 Failure Detector Multiplexer - Large resistor segment bypass transistors place resistor segments that are to be measured near the Vdd rail potential in order to allow simple voltage to current conversion with a 100KΩ well resistor. Also, note that the stress current is limited by a current mirror which doubles as a test current regulator.

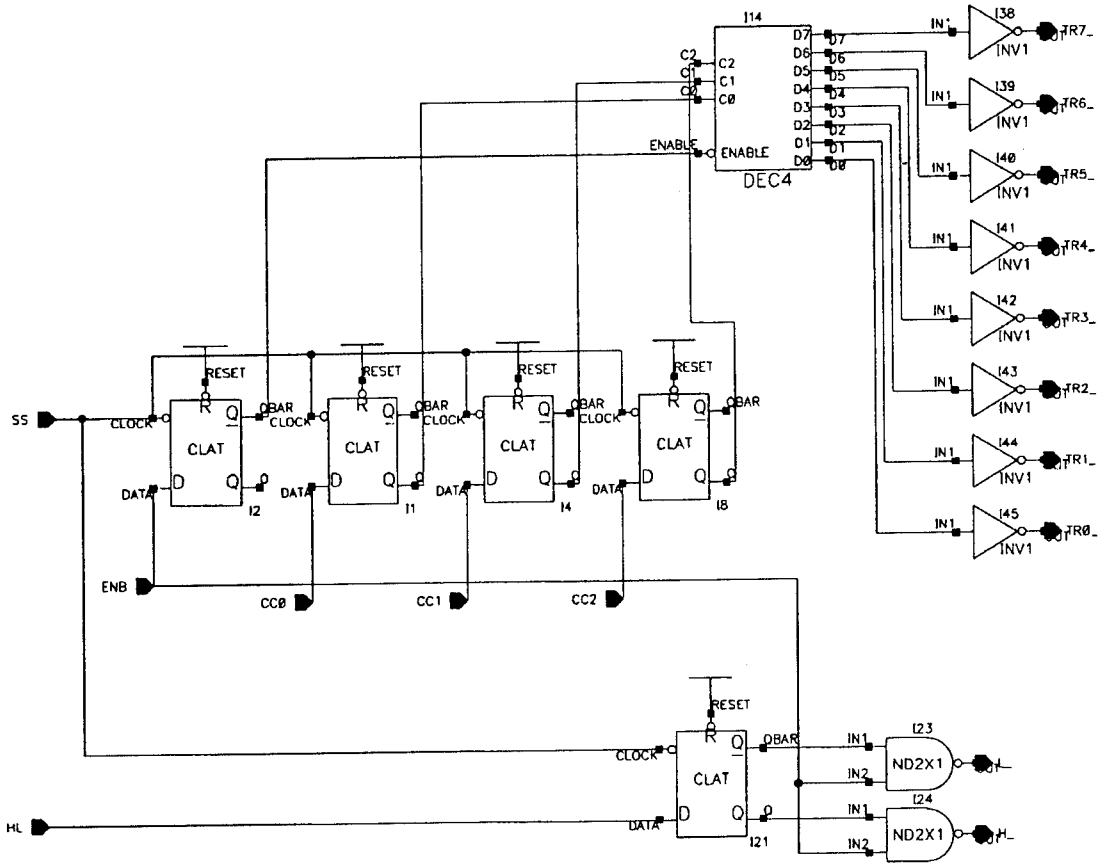


Figure D8: Version 2 Multiplexer Address Latch and Decoder Logic Diagram - Requires only an additional flip-flop plus two NAND gates compared to Version 1.

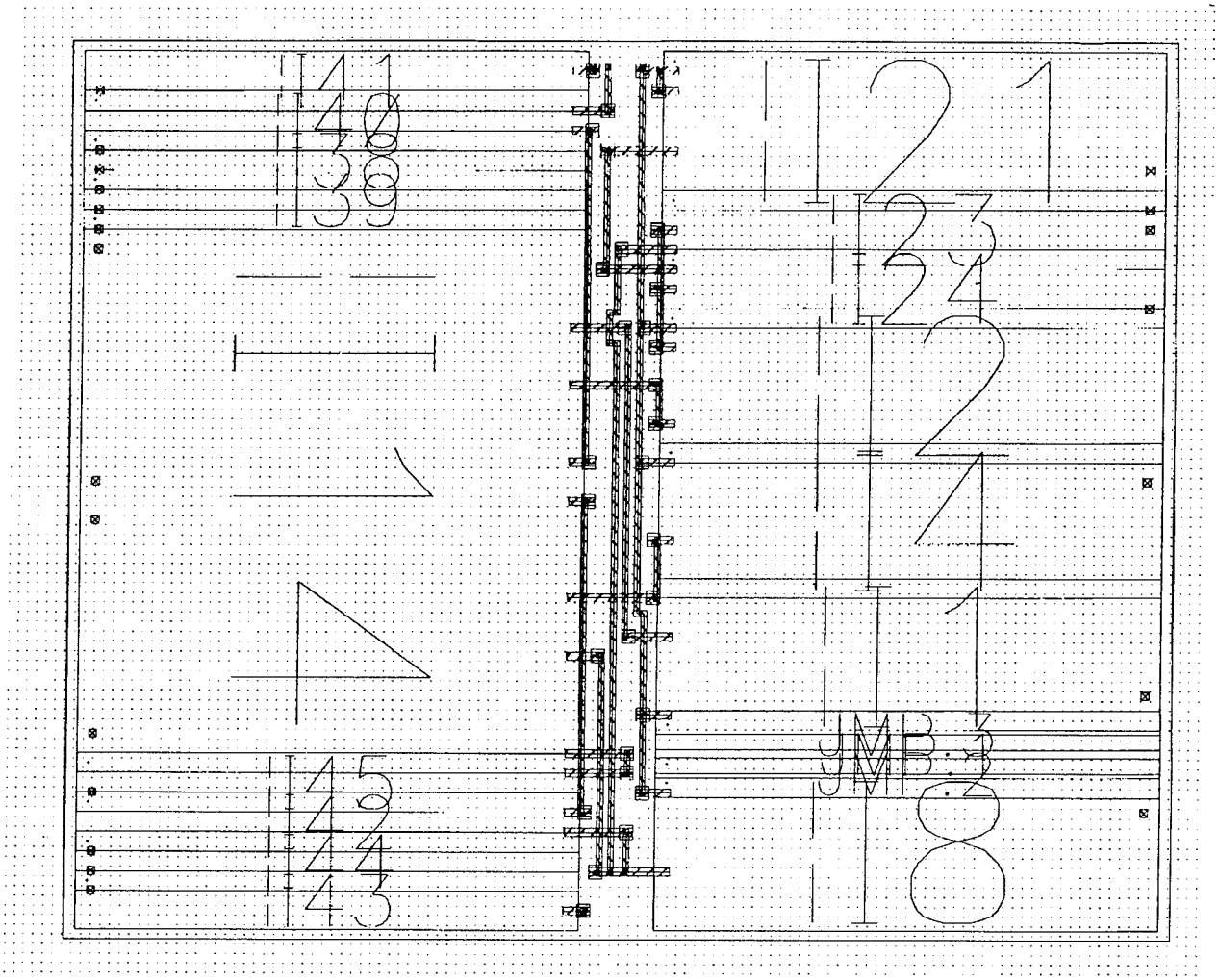


Figure D9: Version 2 Multiplexer Address Latch and Decoder Layout - Shows standard cell placement and cell interconnect. Standard cell layouts are omitted.

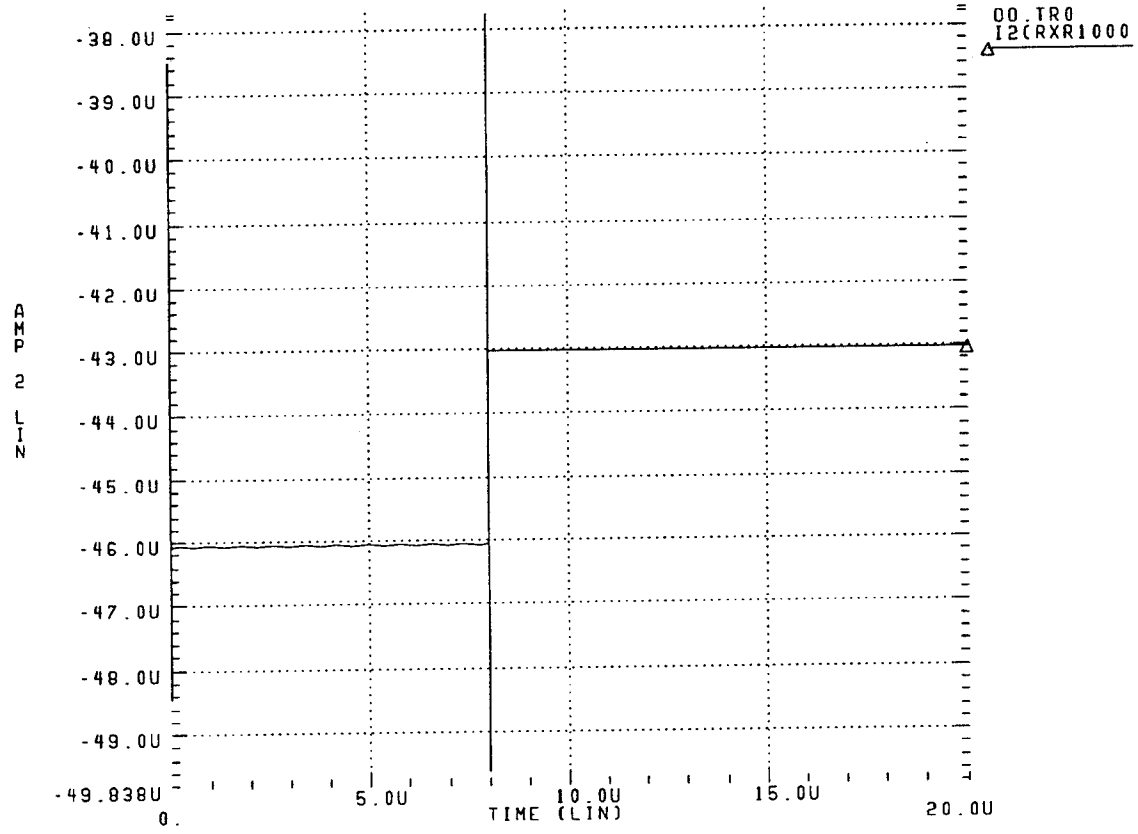


Figure D10a: SPICE simulation of R1 resistance measurement before stress.

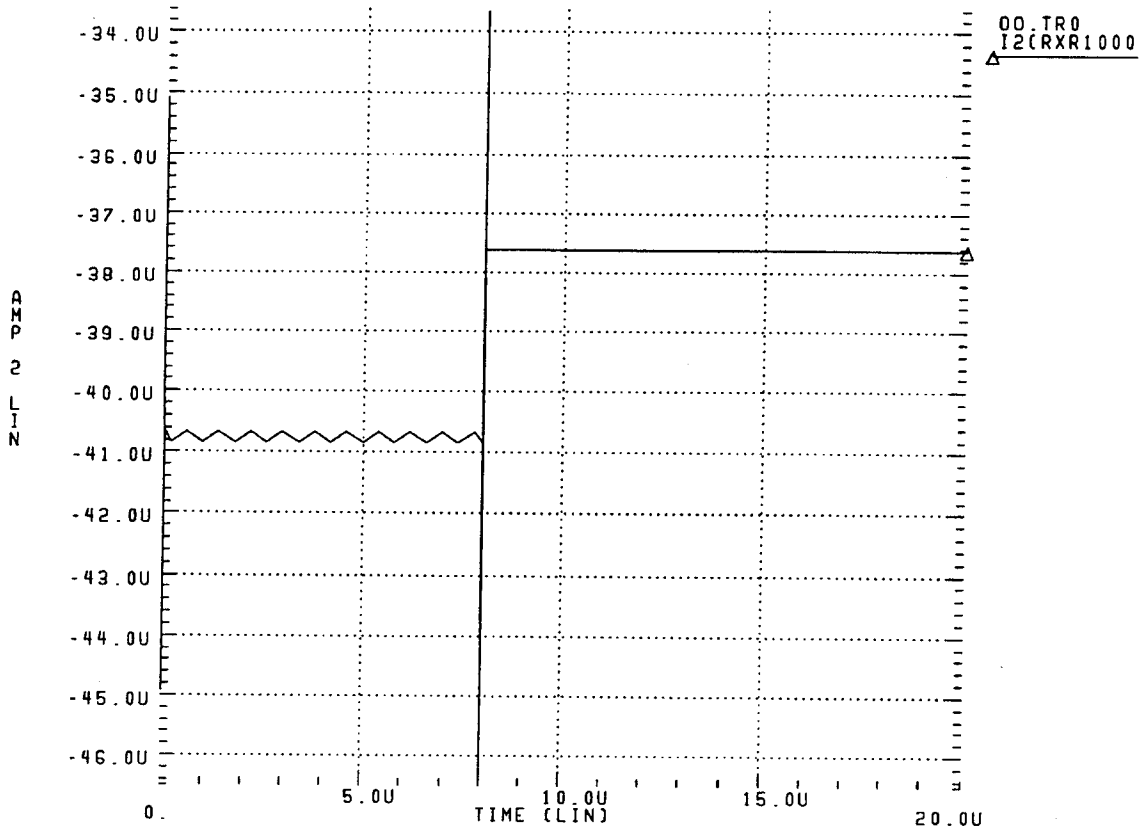


Figure D10b: SPICE simulation of R7 resistance measurement before stress.

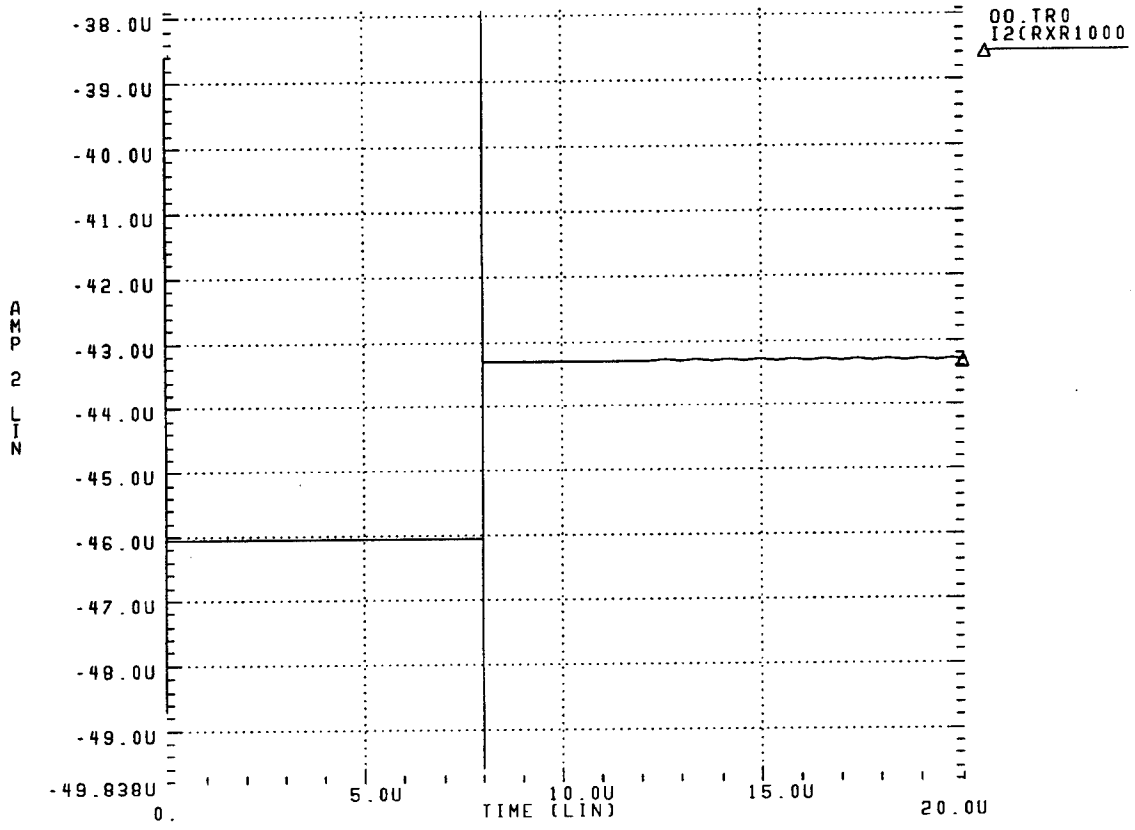


Figure D11a: SPICE simulation of R1 resistance measurement after stress caused resistance increase.

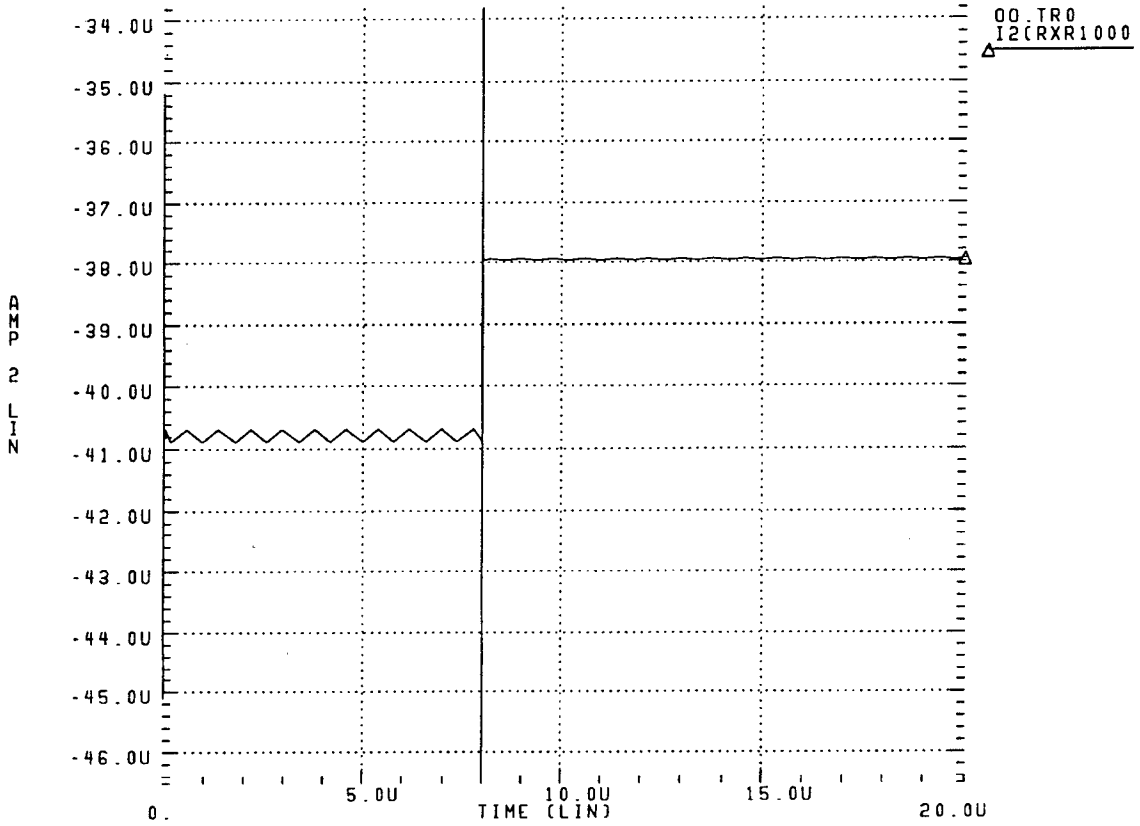


Figure D11b: SPICE simulation of R7 resistance measurement after stress caused resistance increase.

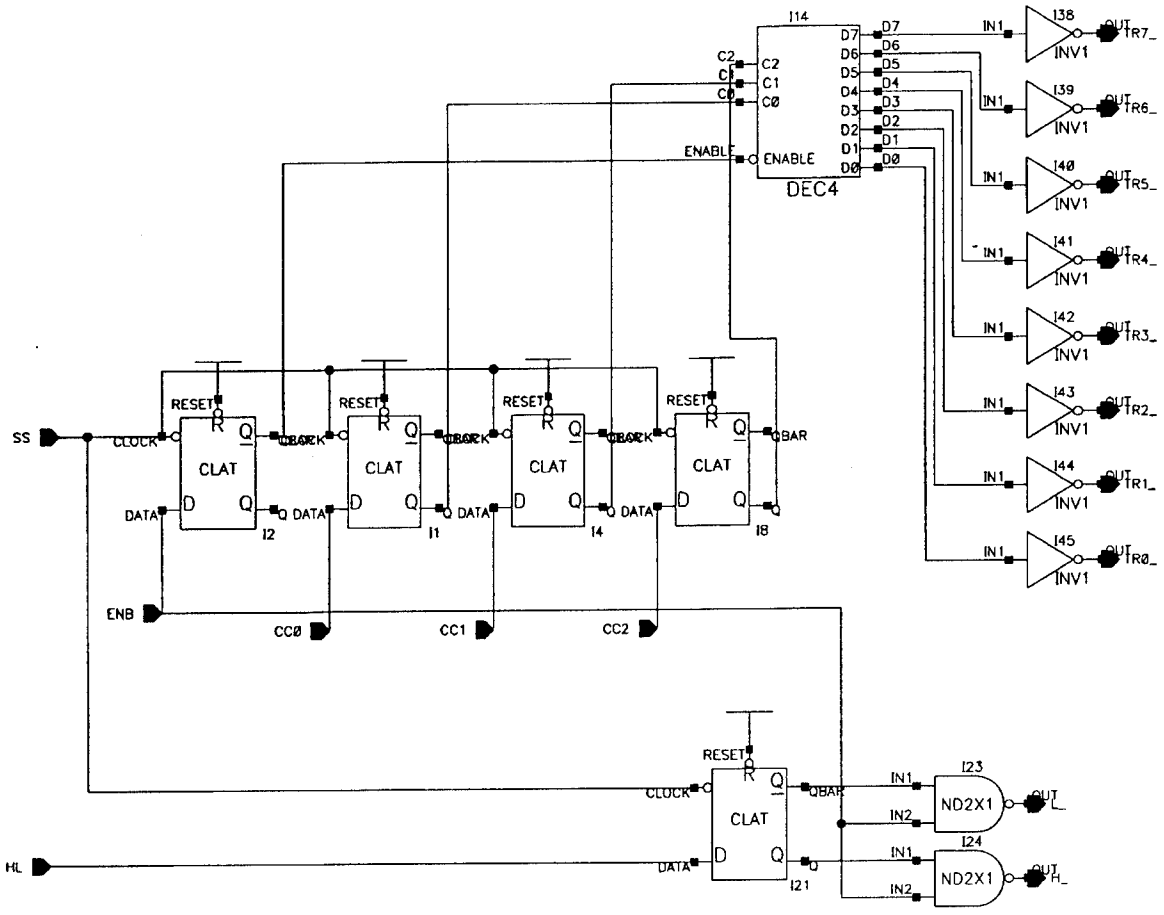


Figure D12: Version 2 Multiplexer Address Latch and Decoder Logic Diagram - Requires only an additional flip-flop plus two NAND gates compared to Version 1.

Appendix E

Boundary Scan and Finite State Machine

Boundary Scan and Finite State Machine

The Boundary Scan logic diagram is found in Figure E1. It is constructed from CMOSN cells and is a direct implementation of the basic boundary scan cell found in the IEEE Std. 1149.1-1990. The layout of the cell is in Figure E2. Logic simulations performed on this design indicate that it performs the intended function. No SPICE simulations were run because we feel that the CAD system logic simulation is adequate for this standard cell based design.

The Finite State Machine (FSM) is primarily used for measuring the current controlled oscillator frequency by gating its output into a 16-bit counter. The logic diagram of the FSM is found in Figure E3b. The FSM with the 16-bit counter is in Figure E3a, which unfortunately is rather difficult to read at this scale.

Logic simulation results of the in the form of timing diagrams FSM are found in Figures E4, E5, and E6. The simulation figures are of three critical regions of operation: 1)Initialization. 2) Steady State. 3) Commanded Reset by CLKB. Output from the 16-bit counter is not shown because there is little that can be learned from the graphics that can not be gathered from knowing that it functions correctly.

Initialization is executed at chip power-up. It differs little from the operation of the FSM at update intervals indicated by the execution of CLKB. The graph in Figure E4 shows the first 150ns. of operation after initialization.

Steady state is the condition in which CLKA is continuously present during operation of the self-stressing circuits at times when there is a state change or a data collection operation. At intervals during steady state the FSM samples the Current Controlled Oscillator frequency and saves the count in the boundary scan cells that are connected to the 16-bit counter. Correct operation of this count save is shown by the presence of DS and DSBAR. After frequency data is saved the 16-bit counter is reset (RST) and counting begins again when GATE is high. The graph in Figure E5 shows the time interval between 20.5μs and 21.0μs.

Commanded reset occurs when the off-chip boundary scan controller sends a CLKB to extract saved data from the self-exercising cells and to update the status of the self-stressing cells. When this occurs the time interval for the GATE signal may be less than required for correct frequency determination, but the correct frequency is contained in the boundary scan cells for the previous count interval. In general the off-chip boundary scan controller will supply the CLKA and will know the exact state of the self-stressing cells at all times. Therefore an aborted frequency count need never occur. The graph in Figure E6 shows the time interval between 40.8μs and 41.3μs.

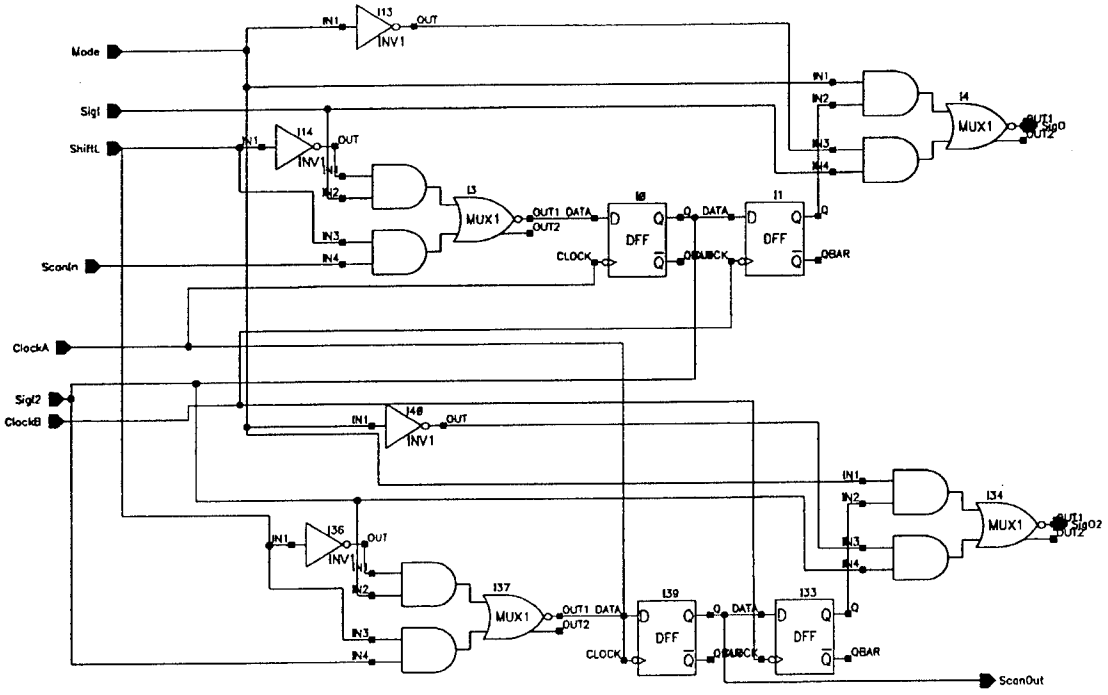


Figure E1: Boundary Scan Logic Diagram - A CMOSN cell library implementation.

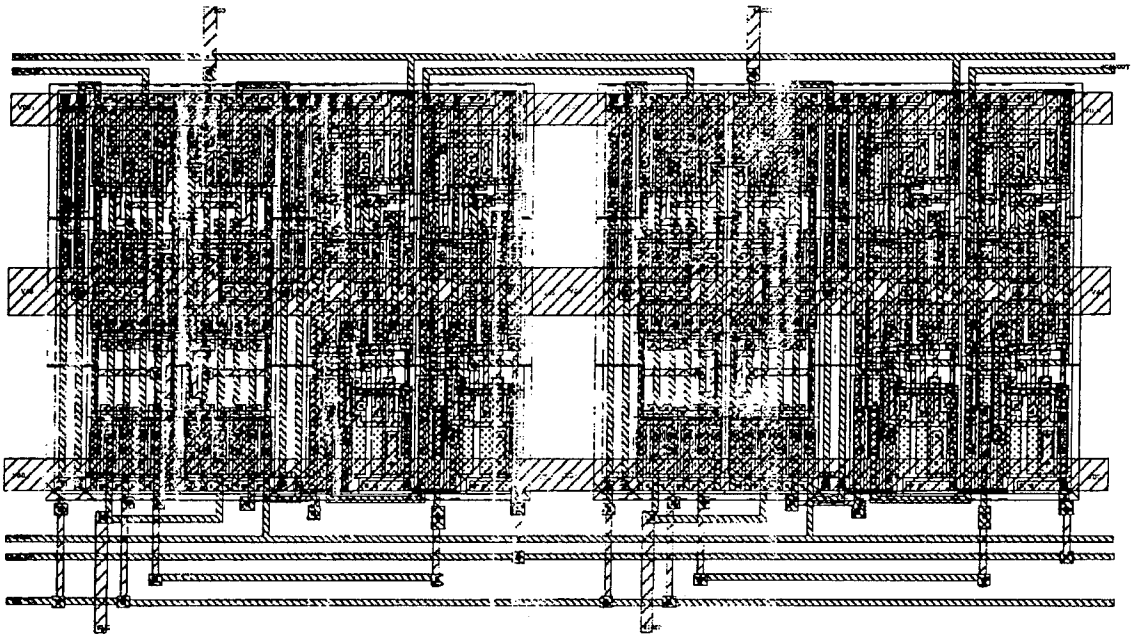


Figure E2: Boundary Scan Logic Layout - Constructed with a double row of cells.

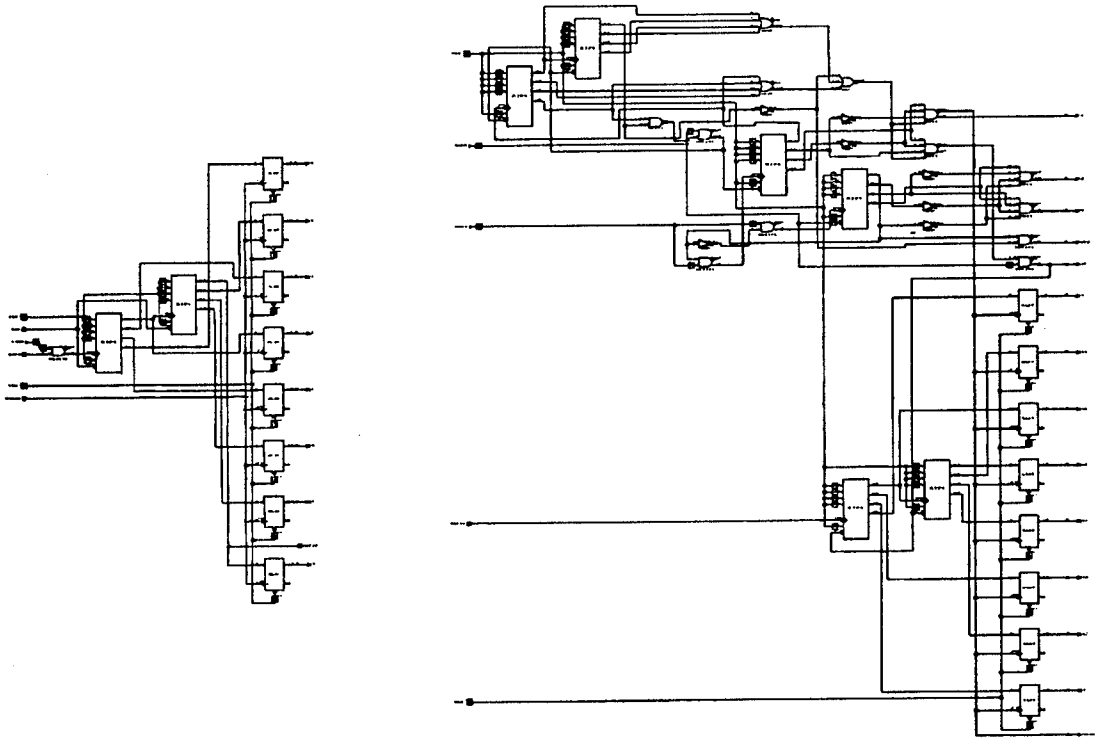


Figure E3a: Finite State Machine with the 16-bit counter logic cells.

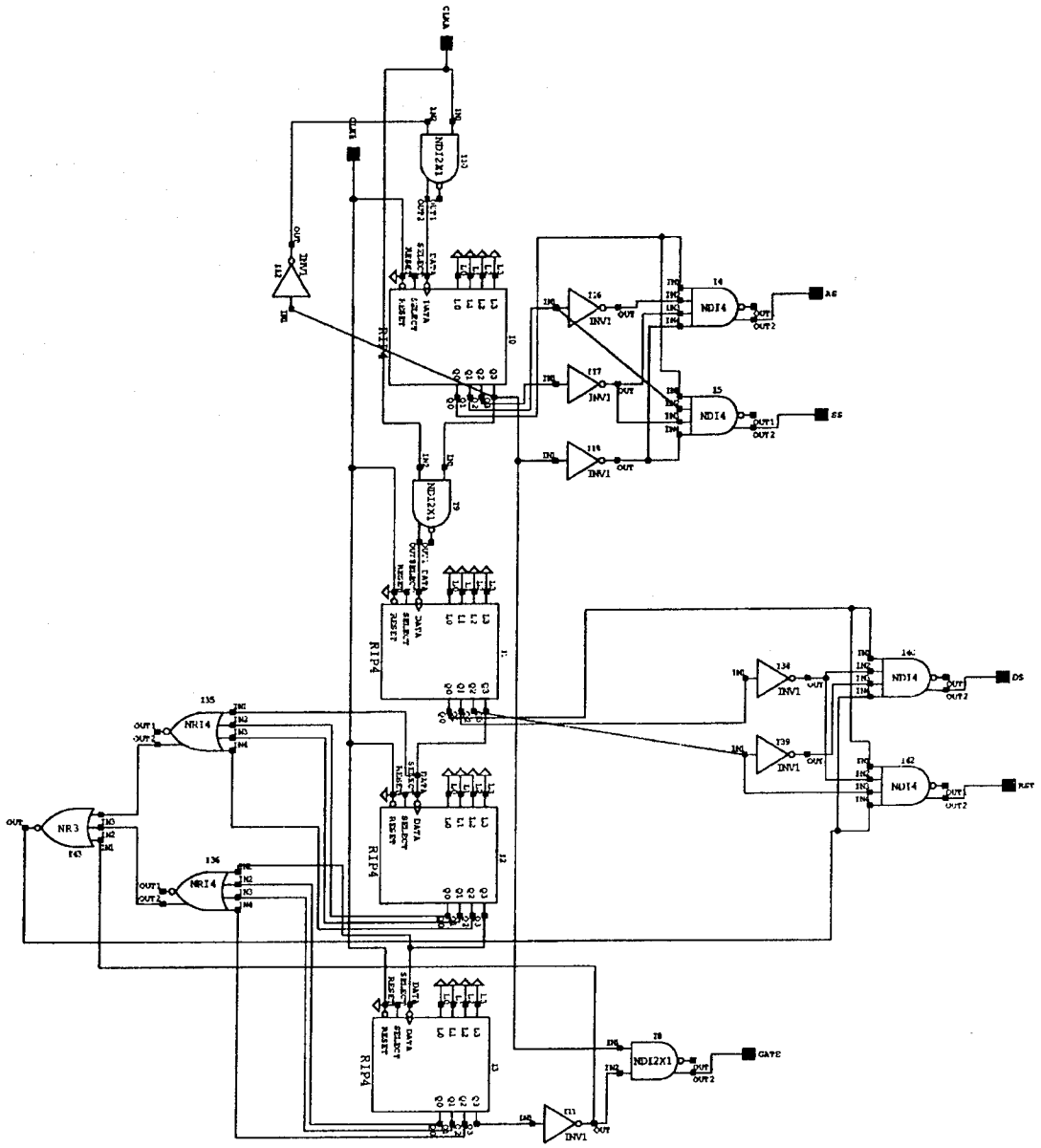


Figure E3b: Finite State Machine Logic Diagram.

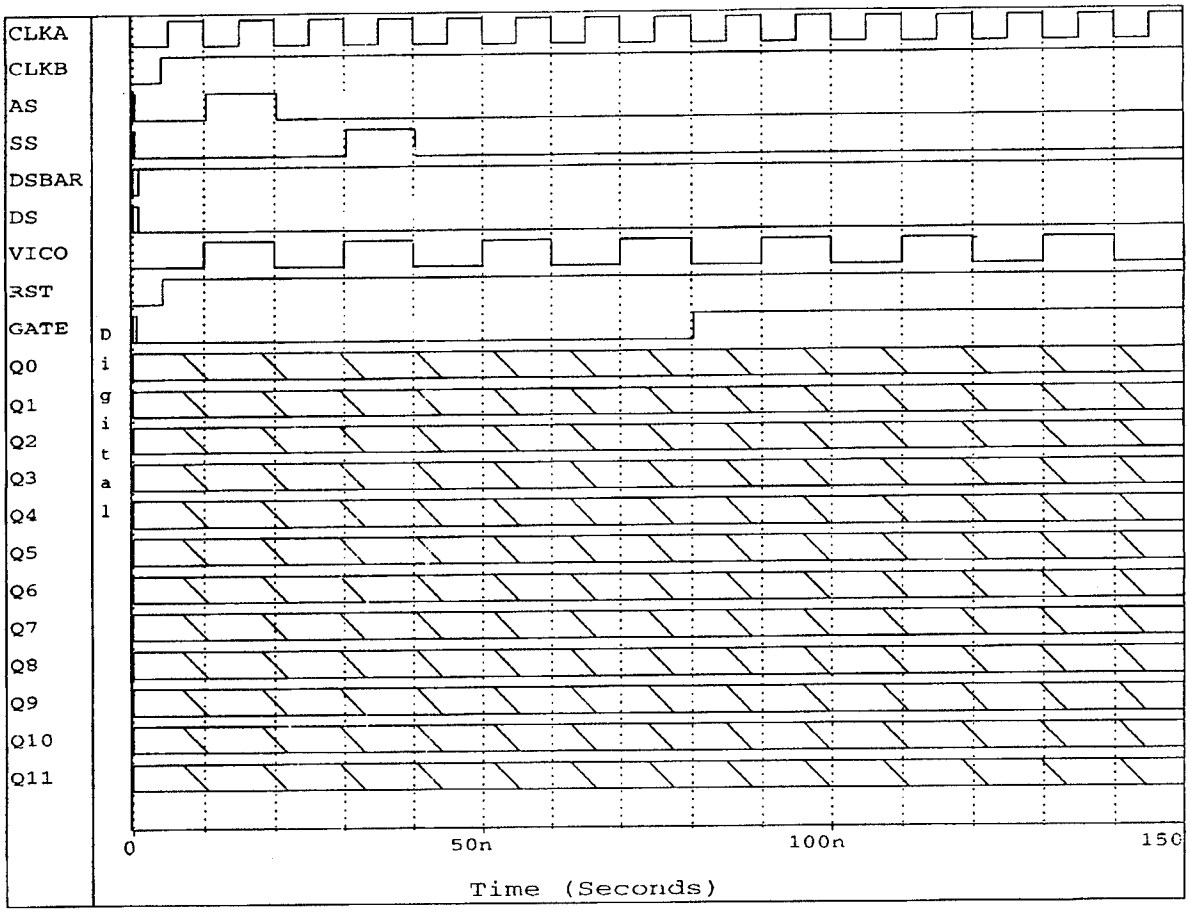


Figure E4: Finite State Machine Logic Simulation - Initialization.

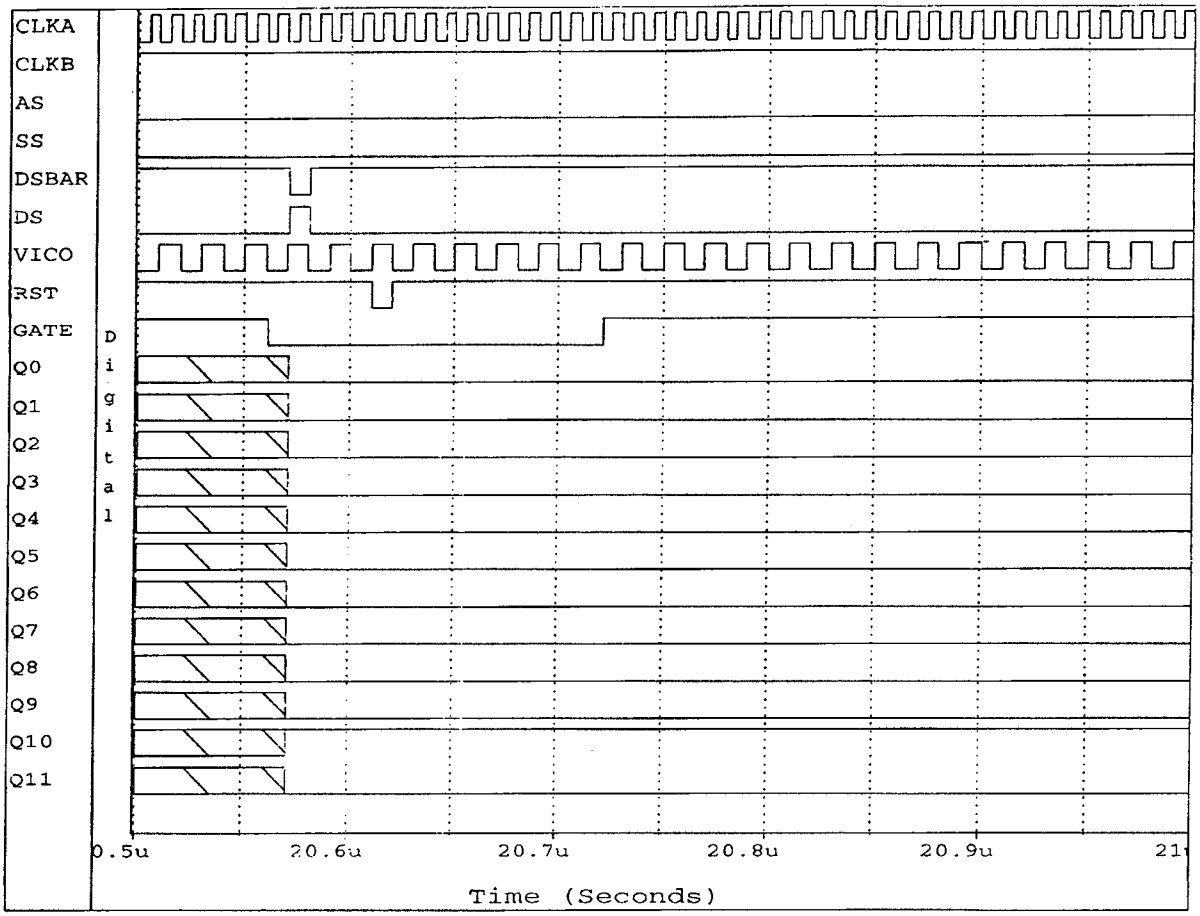


Figure E5: Finite State Machine Logic Simulation - Steady State.

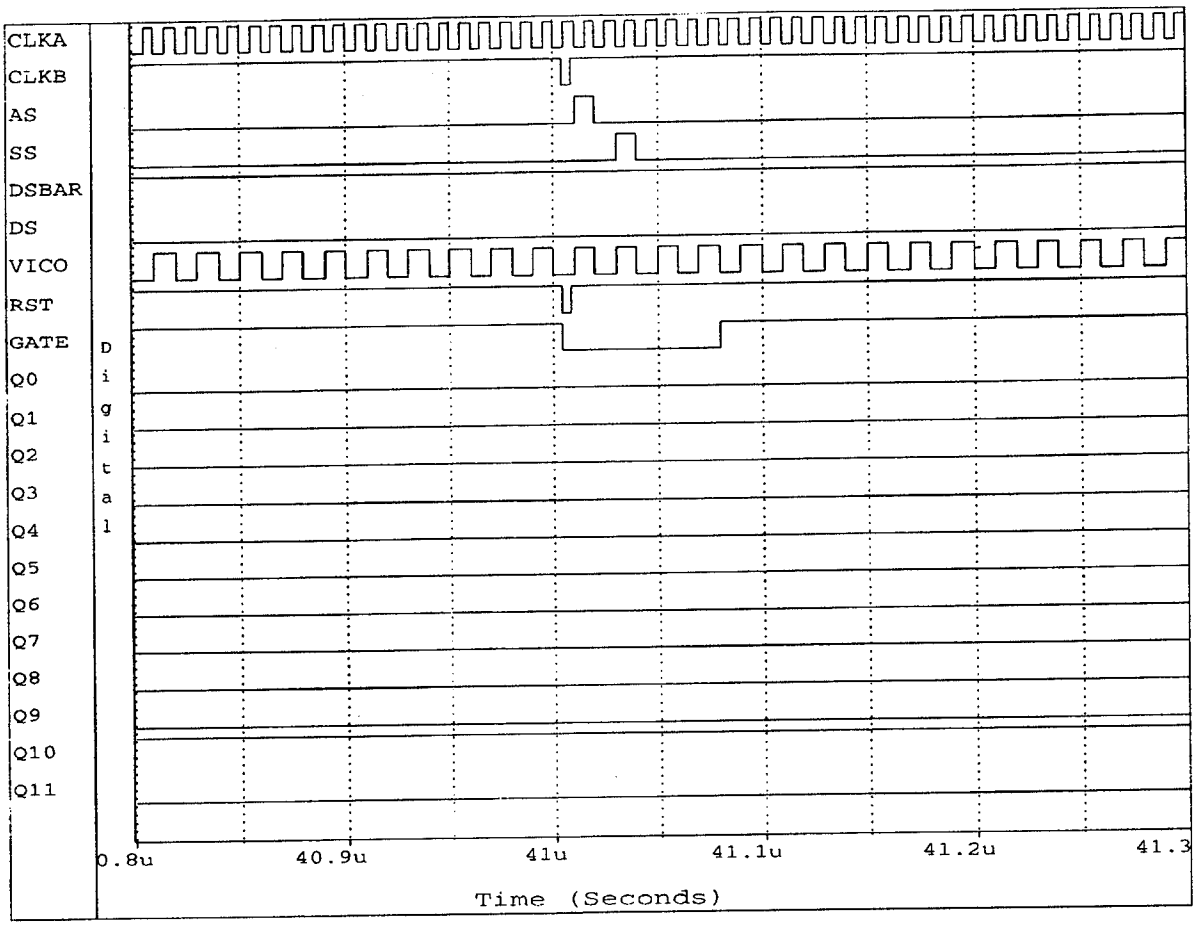


Figure E6: Finite State Machine Logic Simulation - Command Reset.

Appendix F

Test Chip Number 1

Test Chip Number 1

Test chip number 1 layout is shown in Figure F1. This chip was fabricated early in the schedule of this task to determine how well the SPICE simulations agree with a silicon realization of certain key self-exercising cells. In particular we were interested in how well the simulations of the well bias generator compare with the fabricated well generator. In addition there were samples of the basic boundary scan cell, as well as the first version of the hot carrier test circuit that involves the use of a differential pair of N-channel transistors that can be hot carrier stressed in parallel and then tested as a balanced pair in the differential amplifier. A substrate bias generator was included to test the P-well version of this design on a N-well fabrication run. All of the digital elements as well as the I/O pads used in this chip were from the CMOSN cell library, while all of the custom cells were constructed in MOSIS Scaleable CMOS rules. We found that the fabricated chip did not function and spent a great deal of time trying to determine why the simulations and the circuit extractor did not predict non-operation.

After analysis of the chip layout and the chip itself we found that the error was related to the fact that there were two different sets of design rules involved in constructing the chip. The CMOSN cells were designed with a set of NSA (NSCN) CMOS design rules that are compatible with MOSIS fabrication when a value of lambda is chosen that is slightly different from what would be commonly used with the MOSIS SCN CMOS rules. By selecting a lambda of 0.8μm for the CMOSN cells and a lambda value of 1.0μm for the circuits designed in MOSIS SCN rules the two sets of layouts would scale to the correct geometry for the 2.0μm CMOS fabrication line that fabricated the chip. Unfortunately this split requirement for different values of lambda worked fine in the CAD system but when the CIF file was generated the correct values of lambda were not correctly included in the final CIF file for the chip. The result was that the chip has some design rule violations at the mask level that resulted in all of the CMOSN cells being non-functional.

Since there was no way to communicate with the digital circuitry on the chip it was impossible to test the chip. Since so much time was spent in this debug process, there was not enough time to design, simulate and design rule verify a second ship that could possible be fabricated in the time that remained on this task. Rather than risk being unable to test a second chip, we chose to concentrate on the problem of being able to create an A/D conversion function that would operate satisfactorily in a single voltage power supply situation.

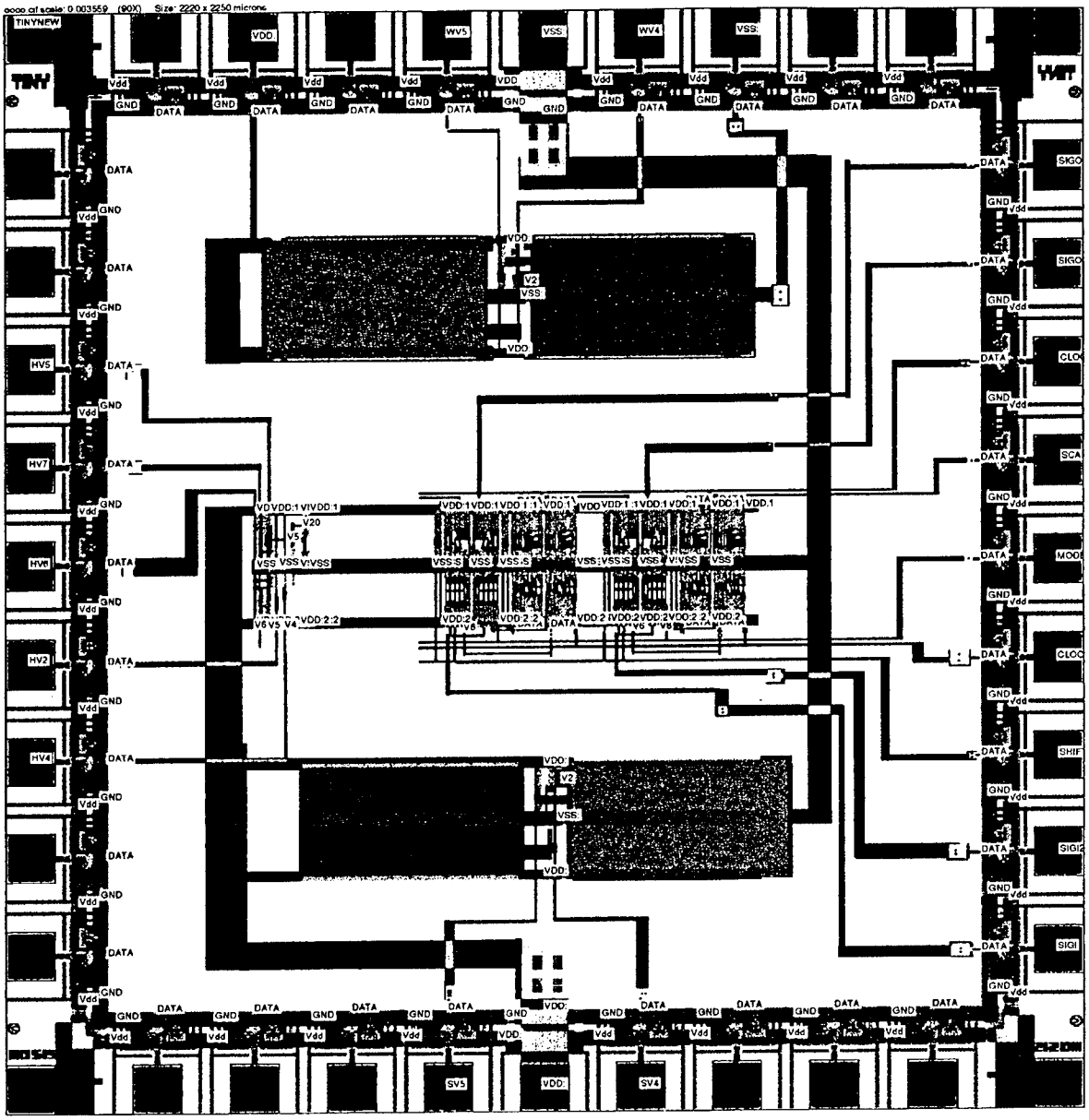


Figure F1: Test Chip Number 1 - Full Chip Layout Diagram.

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